



**Virtex-5 SXT Platform  
Technical Backgrounder  
February 5, 2007**

**Introduction**

The Virtex™-5 SXT platform is the latest addition to the Xilinx XtremeDSP™ portfolio with three new device options that meet the ultra-high digital signal processing (DSP) bandwidth and lower system-cost requirements of next-generation wireless, military/aerospace and multi-media video applications. With shipment of the SXT platform, the third of four 65-nanometer (nm) Virtex-5 FPGA platforms, Xilinx FPGAs now deliver DSP performance up to 352 GMACs at 550MHz while consuming 35 percent less dynamic power as compared to previous 90-nm generations. The Virtex-5 SXT platform is also the industry's first DSP-optimized FPGA family to offer serial connectivity with low-power transceivers that operate up to 3.2 Gbps.

In addition to boosting logic performance with 65-nm [ExpressFabric™](#) technology, all Virtex-5 FPGAs incorporate user-configurable [DSP48E slices](#) — the next step in the evolution of the multiply-accumulate (MAC) functional block. These DSP engines are performance tuned to execute MAC operations at frequencies up to 550 MHz. The inherent ability of FPGAs to implement highly parallel architectures enables astounding DSP performance (two orders of magnitude higher than discrete DSP processors) with the lowest cost and power per channel for complex DSP systems.

Virtex-5 SXT devices range in logic density from 35,000 to 95,000 logic cells along with 192 to 640 dedicated DSP48E slices. With up to 11.6 Mbits of embedded BlockRAM and DistributedRAM, these devices also offer the highest memory-to-logic ratio for efficiently implementing memory-intensive functions typically required for DSP applications in the video processing and medical imaging markets.

Virtex-5 SXT FPGAs incorporate the low-power [RocketIO™ GTP transceivers](#) (<100mW typical @ 3.2 Gbps) and built-in PCI Express® endpoints and Ethernet MAC blocks introduced in Virtex-5 LXT platform devices. Both platforms offer support for all major serial I/O protocols (PCIe™, CPRI, OBSAI, SRIO, GbE, and XAUI) to provide the lowest power solutions for building high-speed, high-bandwidth connections between chips, boards, and boxes.

**Addressing the DSP Performance Gap**

Among the more significant market dynamics driving the need for FPGAs in DSP applications is the growth in algorithmic complexity over the last two decades. Indicative of the problem facing fixed-architecture processors such as DSPs and general purpose processors (GPPs), inherent architectural inefficiencies for these devices constrain their performance to a point well below the theoretical limits established by Moore's Law.

Conversely, algorithmic complexity has been growing at an accelerated rate, due in large part to the demand for communications systems that push the upper limits of data transmission efficiency as defined by Shannon's Law (see Figure 1). Advanced techniques such as Reed-Solomon codes and, more recently, Turbo codes come much closer to reaching the theoretical Shannon limit<sup>1</sup>, but at a cost of high computational complexity.

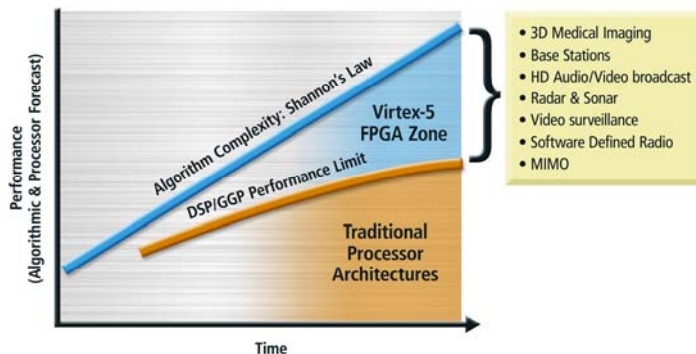


Figure 1 - FPGAs fill the performance gap created by the growth in algorithmic complexity and the inefficiency of fixed-architecture processors

This leaves an ever widening gap between today's algorithmic performance requirements and processor performance. As a result, designers must consider extending their design repertoire (their [DSP Worldview](#)) beyond fixed architecture processors to include the FPGA.

FPGAs are well suited to fill the performance gap because they offer the extremely high-performance signal processing capabilities made possible by their inherent parallelism, while minimizing risk due to changing standards, specifications and even environmental conditions by enabling design migration through their flexible architecture.

Market research firm Forward Concepts estimates the high-performance DSP market at \$2B and forecasts that this segment will grow at 20 percent CAGR between 2005 and 2009. The firm predicts much of that growth will come from increased adoption of programmable devices.

### High-end DSP Market Requirements

FPGAs overcome a composite of market dynamics and challenges. DSP developers demand performance, not just as raw horsepower for DSP operations, but also in terms of greater algorithmic efficiency, along with the higher memory and IO bandwidth required to handle the needs of the infrastructure markets. The challenge is compounded by the need to reduce overall power consumption, simplify power management, and reduce CAPEX and OPEX. Achieving these goals requires lowering bill of material (BOM) costs through integration, lowering design

<sup>1</sup> The Shannon limit of a communications channel is the theoretical maximum information transfer rate of the channel for a given noise level.

costs, and managing risk, complexity and change. Virtex-5 FPGAs provide the best overall solution to address these requirements.

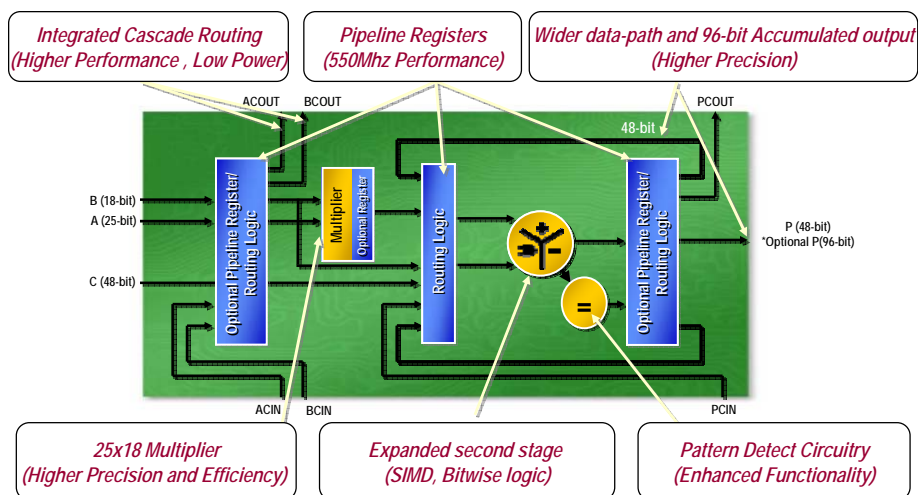
## Delivering the Highest DSP Performance

DSP performance requires a high-performance DSP engine, along with an efficient way to get data in and out of the processing hardware. Virtex-5 SXT FPGAs provide industry-leading value in both of these areas.

### DSP48E slices for maximum DSP performance

The key to the Virtex-5 DSP capabilities is the DSP48E slice (Figure 2). This second-generation DSP MAC engine incorporates a number of enhancements to the innovative DSP48 architecture introduced in the Virtex-4 FPGA family<sup>2</sup>. The DSP48E slices provide improved flexibility and utilization, lower power consumption and increased maximum frequency. The Virtex-5 SX95T device has 640 built-in 18x25 DSP48E slices, delivering up to 352 GMACs performance, augmenting the 30 percent increase in logic performance inherent to the 65-nm ExpressFabric architecture of the Virtex-5 family.

Figure 2 - Virtex-5 SXT DSP48E Slice



The DSP48E slice supports over 40 dynamically controlled operating modes, including: multiplier, multiplier-accumulator, multiplier-adder/subtractor, three input adder, barrel shifter, wide bus multiplexers, wide counters, and comparators.

The key improvements incorporated in the DSP48E slice include:

- **Increased multiplier width:** The Virtex-5 DSP48E slice increases multiplier size to 25x18 (vs. 18x18 in Virtex-4). Matched with a wider data path and a 96-bit accumulated output to enable higher precision, single-precision floating point operation, the DSP48E slice consumes fewer resources for high-precision filter operations.

<sup>2</sup> First-generation DSP48 slice described in [UG073: XtremeDSP for Virtex-4 FPGAs User Guide](#)

- *Enhanced cascade routing:* Multiply-accumulate is the key operation underlying most digital filters. FPGAs with built-in multiplier blocks enable DSP designers to achieve high performance by implementing dedicated hardware for wide filters. Traditional FPGA architectures require coupling available multiplier blocks to inefficient adder-tree structures. Virtex DSP slices break through these performance bottlenecks with dedicated routing resources that enable the construction of efficient adder-chain architectures. This approach also reduces power consumption by eliminating routing and logic resources.
- *Independent C registers:* The 90-nm Virtex-4 family provides one C register input per DSP tile (two DSP48 slices). In the Virtex-5 family, the number of signals available for the DSP48E Slice has increased, allowing for independent C registers, which offers more flexibility and easier implementation of DSP algorithms.
- *Expanded second stage:* The Virtex-4 DSP48 slice provides a multiplier stage followed by an adder stage to enable efficient multiply-accumulate execution. In the enhanced Virtex-5 DSP48E slice, the second stage has expanded to an arithmetic logic unit (ALU) that supports bitwise XOR, XNOR, AND, OR, and NOT functions. In addition to this, the DSP48E slice includes built-in pattern detection circuitry.
- Advancing to the 65-nm process node enables Xilinx to increase the speed of the DSP48E slice up to 550 MHz, up from 500 MHz operation in Virtex-4 FPGAs.

The DSP48E slice enables the creation of efficient adder-chain architectures for implementing high-performance filters and complex math functions. The improvements offered in the DSP48E slice reflect the continued commitment by Xilinx to delivering the industry's premier DSP platform to the high-performance DSP engineering community.

### ***Higher bandwidth***

In addition to fast logic execution, a high-performance system requires the ability to move large amounts of data in and out of the processing element. Virtex FPGAs offer three complimentary approaches for building efficient memory structures:

- Distributed RAM built from memory cells in the look-up-table (LUT) logic structures support the implementation of 64-bit shift-registers
- Embedded BlockRAM structures offer up to 8.8 Mbits of memory in 36-Kbit blocks
- Xilinx [SelectIO](#)<sup>™</sup> technology enables high-bandwidth interfaces to the latest memory high-speed memory devices

Since the BlockRAM structures are alongside the DSP48E slices, they provide an ultra-high-bandwidth means of delivering data to filter architectures. The SXT platform offers up to 8.8 Mbits of 550MHz BlockRAM plus 1.5 Mbits of 550 MHz distributed RAM, delivering a maximum aggregate memory bandwidth of 58 Tera-bits/sec, the highest in this class of DSP performance.

Designers are rapidly adopting serial interface techniques to address increasing chip-to-chip and board-to-board bandwidth requirements. Virtex-5 FPGAs simplify interfacing with built-in serial connectivity. The SXT platform has 16 low-power 3.2 Gbps RocketIO transceivers that support

industry-standard protocols such as CPRI/OBSAI, HD/SDI, Serial RapidIO, PCI Express® and Gigabit Ethernet among others. PCI Express and Gigabit Ethernet are supported with built-in protocol blocks and interfaces.

### Reducing Power Consumption

The Virtex-5 SXT platform helps designers meet tight power budgets by reducing power consumption while delivering the highest DSP performance without compromise or tradeoffs. The 65-nm Virtex-5 SXT platform is built on a second-generation triple-oxide technology that uses ultra-thin gate oxides for the highest-performance transistors, a medium-thickness oxide for configuration and routing circuitry (which can accommodate a tradeoff of performance for lower leakage current) and a thick oxide in I/O structures (to stand up to higher voltages). This keeps static power on par with the 90-nm Virtex-4 family. Additionally, the 65-nm ExpressFabric architecture reduces dynamic power consumption as compared to the previous generation.

The 65-nm triple-oxide technology also makes DSP48E slices more power efficient than their Virtex-4 counterparts, drawing only 1.4mW/100 MHz at a toggle rate of 38 percent – a 40 percent reduction from previous-generation slices. Power reduction also comes from other Virtex-5 hard IP and the industry’s lowest power transceivers, which consume <100mW typical per channel at their maximum line rate of 3.2 Gbps. All of these result in a lower power budget and all its associated benefits – higher reliability, fewer power supplies, savings on fans and heat sinks, etc. Figure 3 shows typical power reduction Virtex-5 SXT offers over Virtex-4 FPGAs on a WiMax digital front end design:<sup>3</sup>

Design	Virtex-4 Power (W)	Virtex-5 Power (W)	% Decrease
DUC+CFR	0.858	0.552	35.6
DDC+AGC	0.740	0.478	35.4
Total DFE	1.598	1.030	35.5

Figure 3 - WiMax digital front-end (DFE) design power reduction example

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<sup>3</sup> DUC: Digital Up Conversion, CFR: Crest Factor Reduction, DDC: Digital Down Conversion, AGC: Automatic gain control

## Complete Design Environment

An essential factor in helping customers design with the Virtex-5 SXT platform is the degree to which the design tools accommodate hardware, software and algorithm developers. Since the launch of the XtremeDSP Initiative in November of 2000, Xilinx [DSP design tools](#) have evolved to provide system modeling, algorithmic development and exploration, automatic generation of test benches, design verification and debugging, and HDL generation and simulation, all from within one design environment. Whether the designer prefers working with C/C++, MATLAB®, Simulink®, HDL, or any combination of these, Xilinx tools provide fast and efficient access to the full power of the FPGA. This is illustrated in Figure 4 below.

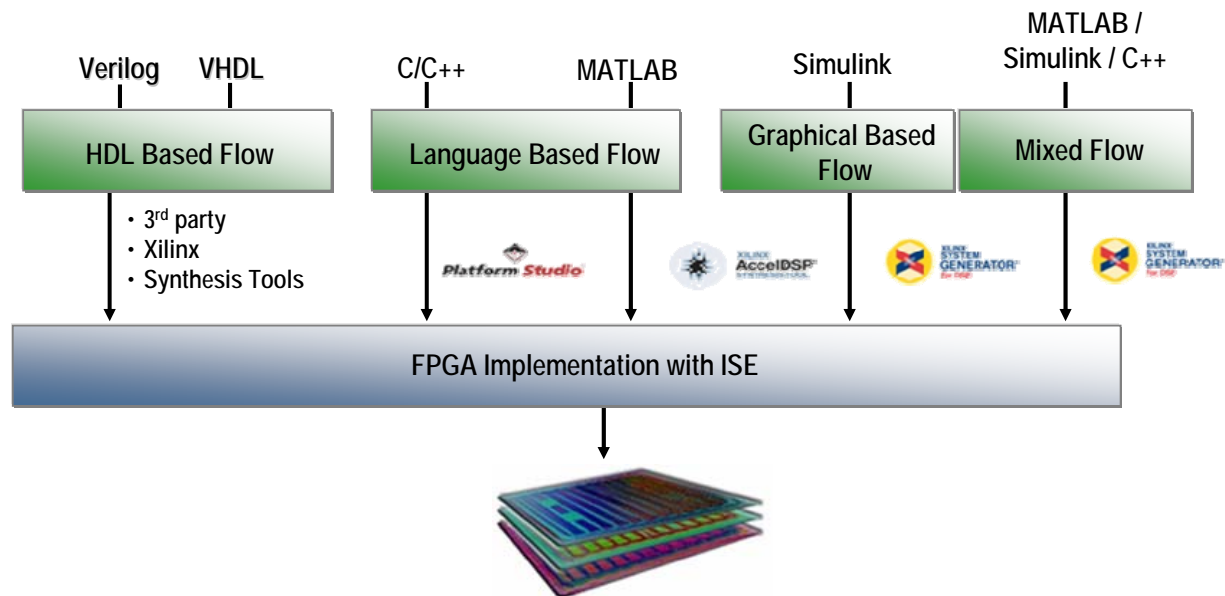


Figure 4 - Complete design environment

## Lowering Costs through Integration

FPGAs allow designers to integrate other components they will need in their system. High-end FPGAs like the Virtex-5 SXT devices integrate a substantial amount of functionality as embedded hard IP (e.g., dedicated DSP slices, PCIe endpoint blocks, low-power transceivers, BlockRAM). In addition, Xilinx provides an ecosystem of IP and design services to integrate DSP functionality as logic or dedicated DSP slice implementations. This integration helps to lower BOM costs, reduce board space, reduce design complexity, and lower power with all the advantages of using a single vendor source.

Figure 5 illustrates how Virtex-5 SXT FPGAs can integrate the functionality of six different ICs (multiple ASSPs and two discrete PHY chips) and still consume only 36 percent of a single Virtex-5 SX35T at 63 percent lower BOM costs and 46 percent lower power consumption. The design used is a Single-Sector 15MHz (3 carrier) UMTS with Diversity Receiver.

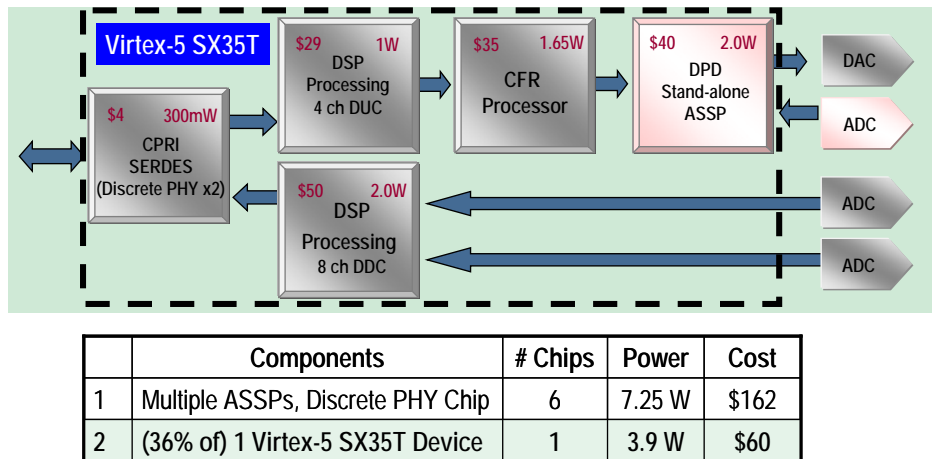


Figure 5 - Cost and power reduction through integration

## Summary

It is no accident that Xilinx FPGAs serve an increasingly vital role in the design and development of today's most demanding DSP systems. After two decades of research, engineering and close collaboration with hundreds of DSP customers, Xilinx FPGAs have evolved into highly valued DSP platforms that stand without peer, delivering the extreme in performance, flexibility, time to market, and product longevity while reducing overall system costs and power consumption.

Long renowned for their inherent ability to implement highly parallel architectures capable of performing complex algorithms in a single clock cycle, today's FPGAs can deliver literally hundreds of mega-samples per second (MSPS) and GMACS with a single device. At these DSP performance levels, the designer can choose either to lower the clock rate of the FPGA to save power or to implement more channels to lower system cost and reduce BOM.

Though certainly compelling, such cost/performance advantages mask other values – flexibility, time to market, and product longevity – that for some promise equally compelling reward. High-growth markets like the communications, MVI (multimedia, video and imaging) and defense industries – all of which depend heavily on high-performance DSP technologies – are in a constant state of flux. Changing standards, changing market demands, changing customer requirements, changing economies, and changing competitive landscapes create substantial business opportunities for companies that can keep pace through innovation and flexibility. For a growing number of system architects and DSP designers, the FPGA is the platform of choice.

Virtex-5 SXT FPGAs deliver the highest aggregate DSP performance (up to 352 GMACs) and are ideal for DSP-processing or co-processing applications. The reconfigurable nature of FPGAs provides the flexibility to quickly construct and refine the architecture to create an ideal implementation for a newly developed algorithm. Additionally, Virtex-5 SXT FPGAs allow designers to integrate other system components (e.g., serial transceivers, PCI Express interfaces, glue logic and low-rate control tasks), thereby reducing overall system cost. Ultimately, the new Virtex-5 SXT platform effectively raises the bar for DSP by providing higher algorithm performance, better power efficiency and lower system cost for a broader range of high-end applications.