The Ultimate System Integration Platform

Low-Power Transceivers
Built-in PCIe & Ethernet
352 GMACS DSP
65nm ExpressFabric

VIRTEX-5 FPGAs
THE WORLD’S FIRST
65nm FPGA

One Family—Multiple Platforms
The Virtex™-5 family of FPGAs offers a choice of four new platforms, each delivering an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing. Three platforms are available now:

• Optimized for high-performance logic
• Optimized for high-performance logic with low-power serial connectivity
• Optimized for DSP and memory-intensive applications with low-power serial connectivity

Discover how this new family delivers even higher performance, lower power, and lower system cost than previous-generation Virtex-4 FPGAs.

Meet Your Performance Targets Easily
• Achieve a two speed-grade performance gain with new ExpressFabric™ technology
• 550 MHz clocking technology and performance-tuned IP blocks
• 392 GMACs performance from DSP48E slices
• 1.25 Gbps LVDS I/O: up to 600 pin pairs (1,200 I/Os)

Optimize I/O Bandwidth, Power and Cost with Easy-to-Use High-Speed Serial Solutions
• RocketIO™ GTP transceivers deliver 100 Mbps – 3.2 Gbps serial connectivity
• First FPGA with hardened PCI Express endpoint blocks and Tri-mode Ethernet MACs
• Lowest power in the industry: less than 100 mW per transceiver at 3.2 Gbps
• Advanced equalization techniques to drive backplanes beyond 40 feet
• Protocol solutions kits accelerate development

Beat Your Power Budget while Maximizing Performance
• 35% lower dynamic power with 65nm ExpressFabric and power-saving IP blocks
• Reduce serial connectivity power consumption: RocketIO GTP transceivers consume less than 100 mW at 3.2 Gbps

Performance

<table>
<thead>
<tr>
<th>Logic Fabric Performance</th>
<th>On-chip RAM 350 MHz</th>
<th>DSP 32-Tap Filter 350 MHz</th>
<th>I/O LVDS Bandwidth 750 Gbps</th>
<th>I/O Memory Bandwidth 336 Gbps</th>
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<tbody>
<tr>
<td>Virtex-5 FPGAs</td>
<td>1.3x</td>
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<tr>
<td>Virtex-4 FPGAs</td>
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<tr>
<td>Nearest Competitor</td>
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Numbers show comparison with nearest competitor based on competitor’s published datasheet numbers.
Reduce Cost through System Integration with Domain-Optimized Platform FPGAs

- Choose a smaller device: 65nm process shrinks die size and new 6-input LUT increases utilization and efficiency
- Meet aggressive performance targets in the least expensive speed grade
- Reduce part count with built-in, low-power transceivers
- Increase logic efficiency with built-in PCI Express® endpoint and Ethernet MAC blocks
- Select smaller heat sinks, fans, and power supplies enabled by reduced power consumption
- Bring your product to market faster with proven development and verification tools
- Reduce component cost in volume production with Virtex-5 EasyPath™ FPGAs

Finish Your Design Ahead of Schedule

- Achieve FPGA performance goals quickly with ISE™ Fmax technology and PlanAhead™ design analysis tools
- Reach timing closure up to 6x faster with new SmartCompile technology
- Design faster and reduce risk with over 225 pre-verified IP cores
- Reduce debug cycle time with the real-time verification capabilities of ChipScope™ Pro tools
- Build complete embedded processing systems with Platform Studio and Embedded Development Kit
- Implement DSP algorithms in custom-configured hardware with the AccelDSP™/MATLAB™ tool flow
- Accelerate product development with online resources, training courses, and premium support services
- Get Xilinx Productivity Advantage (XPAX) bundles of software, education, support services, and IP cores
- Augment your development team with a worldwide network of Xilinx Design Service (XDS) and partner experts

Solve Signal Integrity Challenges and Simplify PCB Layout

- Second-generation sparse chevron packaging delivers SSO noise and crosstalk benefits, essential for reliable operation of high-bandwidth parallel interfaces (e.g., memories)
- On-substrate bypass capacitors and a unique pinout simplify PCB design, improve power integrity, and reduce system cost
- Built-in serial connectivity reduces pintrace count and eliminates parallel interface design challenges

VIRTEX-5 EASYPATH™ FPGAs

The conversion-free cost-reduction path for volume production.

- EasyPath FPGAs reduce component cost by 30–75% with no risk of conversion, no hidden costs
- Enjoy unprecedented flexibility and fastest turn-around times

### Power consumption and area required to implement a typical design including 8-lane PCIe endpoint

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<thead>
<tr>
<th>Virtex-5 LXT FPGAs (65nm)</th>
<th>Nearest Competitor (80nm)</th>
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<tbody>
<tr>
<td>Static Power</td>
<td>25.18</td>
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<td>User Logic</td>
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<td>PCIe</td>
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</table>

**V5_SXT_broc_Final.qxd 1/5/07 8:04 AM Page 3**
THE ULTIMATE SYSTEM INTEGRATION PLATFORM

65nm ExpressFabric™ Technology
Achieve highest performance, most efficient utilization on 65nm triple-oxide process
- 30% higher speed, 35% lower dynamic power, and 45% less area than the previous generation
- Industry’s first LUT with six independent inputs for fewer logic levels
- Flexible LUTs are configurable as logic, distributed RAM or shift registers
- Advanced diagonally symmetric interconnect enables shortest, fastest routing
- From 30,000 to 330,000 logic cells for system-level integration

550 MHz Clocking Technology
Achieve highest speeds with high-precision, low-jitter clocking
- 12 DCMs provide phase control of less than 30 ps for better design margin
- 6 PLLs reduce reference clock jitter by more than 2x
- Differential global clocking ensures low skew and jitter

The Right Memory for Any Application
Distributed RAM—Small
- Build 256-bit memory per CLB
- 64 bits per LUT

550 MHz, 36 Kbit Block RAM—Medium
- Configure Block RAM as multi-rate FIFO
- Built-in ECC for reliability systems
- Automatic power conservation circuitry

High-Performance External Memories—Large
- ChipSync™ technology for reliable interfaces
- Achieve data rates up to 389 Gbps
RocketIO® GTP Transceivers: 100 Mbps–3.2 Gbps

Implement serial protocols at lowest power
- Flexible SERDES supports multi-rate applications
- Designed to work with integrated PCIe™ and Ethernet MAC blocks
- 77% lower power consumption: less than 100 mW at 3.2 Gbps

Sparse Chevron Packaging Technology

Keep system noise under control and simplify PCB layout
- Unique PWR/GND pin pattern minimizes crosstalk and reduces PCB layers
- On-substrate bypass capacitors shrink PCB area

PCI Express Endpoint Block: x1/x2/x4/x8-lane

Built-in support for ubiquitous serial connectivity standard
- PCI-SIG-verified compliance (on integrators list)
- Works with RocketIO GTP transceivers to deliver full PCIe endpoint function
- Built-in hard IP frees user logic resources and reduces power

Ethernet Media Access Controller: 10/100/1000 Mbps

Connect to the Internet via an integrated tri-mode Ethernet MAC
- UNH-verified compliance
- Built-in hard IP frees user logic resources and reduces power
- Four Ethernet MAC blocks on every Virtex-5 LXT/SXT device
Enhanced Configuration and Bitstream Protection

Reduce system cost, increase reliability, and safeguard your design

- Configure with commodity SPI and parallel flash memory
- Easier partial reconfiguration and smaller frame size
- Greater reliability for in-system reconfiguration with multi-bitstream management
- Protect your designs with 256-bit AES (Advanced Encryption Standard) security

1.25 Gbps SelectIO™ with ChipSync™

Implement industry-standard and custom protocols

- Simplify board design with built-in input delay and new output delay circuits that compensate for unequal trace lengths
- Adaptive delay setting recalibrates automatically to compensate for changing operating conditions
- Interface to popular standards with 1.25 Gbps differential and 800 Mbps single-ended I/O
- Digitally controlled impedance improves signal integrity, reduces component count, and shrinks board size

550 MHz DSP48E Slice

Achieve up to 352 GMACS DSP Performance

- Up to 640 DSP48E slices in Virtex-5 SX95T device
- Enhanced slice with 25 x 18 multiplier and 48-bit adder enables single-precision floating-point math and wide filters with fewer slices
- Configurable for DSP arithmetic, and bit-wise logic
- Enables efficient adder-chain architectures
- 40% lower power consumption: 1.38mW/100MHz at a 38% toggle rate

System Monitor and Analog-to-Digital Converter

Simplify system management and diagnostics

- Fully specified 10-bit, 200k samples/s ADC with programmable monitoring functions (sequencing, averaging, alarms)
- Simplify the implementation and reduce the cost of environmental monitoring
- On-chip temperature and supply voltage sensors
- 17 user-selectable external inputs
- Analog measurements accessible via JTAG at any time

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Implement Parallel Networking and System Interface Standards

SelectIO circuitry, combined with pre-verified IP cores, makes it easy to support all popular interface standards:
- 1.25 Gbps LVDS, 800 Mbps single-ended
- Interface or bridge to virtually any external component
- Support multiple electrical standards in the same device with 35 individually configurable I/O banks
- Design with PCI, RapidIO, XSBi, SP4L, and more
- Configure I/Os to support HSTL, LVDS (SDR and DDR), and more, at voltages from 1.2V to 3.3V

Simplify Source-Synchronous Interfacing

ChipSync technology in every SelectIO block provides precise control over critical timing for high-performance source-synchronous interfaces:
- Achieve performance targets and simplify PCB layout with flexible per-bit deskew
- Synchronize incoming data to FPGA internal clock with built-in Serializer/Deserializer

Build Highest-Bandwidth Memory Interfaces

ChipSync technology and the Memory Interface Generator tool make it easy to build reliable interfaces to the latest high-performance memories, including:

<table>
<thead>
<tr>
<th>Memory Interface</th>
<th>Data Rate (Mbps)</th>
<th>Data Width (# of bits)</th>
<th>Bandwidth (Gbps)</th>
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</thead>
<tbody>
<tr>
<td>DDR SDRAM</td>
<td>400</td>
<td>576</td>
<td>230</td>
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<tr>
<td>DDR2 SDRAM</td>
<td>667</td>
<td>576</td>
<td>384</td>
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<tr>
<td>QDR II SRAM</td>
<td>600</td>
<td>2 x 324</td>
<td>389</td>
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<tr>
<td>RLDRAM III</td>
<td>600</td>
<td>648</td>
<td>389</td>
</tr>
</tbody>
</table>

Accelerate Development with Complete Serial Solutions

Build chip-to-chip, board-to-board, and box-to-box applications quickly and easily:
- Obtain assured compliance with popular standards
- Reduce design time with integrated interface blocks and pre-verified IP
- Implement custom solutions
- Reduce pin/trace count to simplify board design and reduce manufacturing cost
- Start designing with ready-to-use solution kits including protocol-specific characterization reports, boards, and simulation models

Bridge Protocols

Protect your investment by interfacing easily to legacy ASSPs or ASICs:
- Reduce design time with built-in support for PCI Express and Ethernet
- Implement other popular protocols with pre-verified IP
- Connect external peripheral components to any processor with standards-compliant I/O
Implement PCI Express with Reduced Cost, Power, and Complexity

Minimize design risk with hardened PCIe blocks for building next-generation graphics, storage, networking, and I/O devices

- Integrate multiple functions into a single PCIe-enabled FPGA
- Preserve software investment and extend infrastructure life with scalable bandwidth (x1, x2, x4, x8)
- Re-target designs without changing your PCIe interface implementation as your project evolves

Integrate Flexible Embedded Control Processors

Combine high-performance logic with the flexibility of software

Virtex FPGAs provide high-bandwidth I/Os, power-efficient embedded blocks, and high-performance logic fabric. Xilinx offers the MicroBlaze® processor for efficient, flexible implementation of control functions.

Build a processor subsystem tailored to your requirements with Embedded Development Kit

- Start with award-winning Platform Studio tool suite
- Instantiate a customizable 32-bit MicroBlaze soft processor
- Select peripherals from a comprehensive IP catalog
- Create custom peripherals to interface with system I/O

Develop your application using industry-standard software IDE tools from Xilinx or partners

- Choose an RTOS from Alliance Embedded partner offerings
- Create custom hardware accelerators using ESL Ecosystem partner tools
Create Highest-Performance DSP Systems

Increase DSP algorithm performance
• Build single or multi-rate filters for high-sample-rate applications in wireless RF or HD video systems with cascadable DSP48E slices
• Perform fine-granularity data shifting, control, and small bit-width arithmetic functions efficiently in programmable logic fabric
• Free up DSP processor CPU cycles by off-loading algorithmic-intensive tasks to the FPGA co-processor
• Obtain highest memory-to-logic ratio with Virtex-5 SXT platform for efficiently implementing memory-intensive functions in video processing and medical imaging

Optimize DSP power consumption and cost
• Achieve efficient implementation with Xilinx algorithm/IP core support for base functions (e.g. FFT, filters), wireless functions (e.g. DDC, DUC, CFI, DF) or video/imaging functions (e.g. CODECs)
• Use power-efficient Virtex-5 FPGAs in military manpack or handheld software defined radios

Build flexible, high-bandwidth interfaces
• Simplify design with built-in support for PCI Express interfaces
• Obtain complete Xilinx solutions for market-specific interfaces such as CPUIDUSBAl for wireless and HDI/SDI for professional broadcast systems
• Build high-bandwidth interfaces to DSP processors using Xilinx IP and reference designs for Serial RapidIO, VLYNX™, or EMM™ when using FPGAs as DSP co-processors

Increase DSP Design Productivity
• Design using MATLAB™, Simulink™, Verilog, VHDL or C, in any combination
• Simulate and verify your design on the FPGA using high-bandwidth hardware-in-the-loop capability
• Protocol compliance reports
• Device characterization
• Reference designs
• Development boards
• Simulation models
• Pre-verified IP
• Development tools
• User documentation
• Partner solutions

TAKE THE NEXT STEP
Visit us online at www.xilinx.com/virtex5

System Integration Design Example: Video-Over-IP

Accelerate development with ready-to-use solution kits
• Protocol compliance reports
• Device characterization
• Reference designs
• Development boards
• Simulation models
• Pre-verified IP
• Development tools
• User documentation
• Partner solutions

Building on Proven DSP Leadership
The Berkeley Design Technology Inc. (www.bdti.com) 2006 independent technical benchmark analysis concluded that Virtex-4 SX25 FPGAs delivered 2X lower cost-per-channel compared to Altera Stratix-II 2S15 FPGAs for the BDTI Communications Benchmark (OFDM™).
### Notes:
1. A single Virtex-5 CLB comprises two slices, with each containing four Real 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
2. Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new Real 6-input LUT architecture.
3. Number of available RocketIO™ multi-gigabit transceivers (MGTs) for each device/package combination shown in parentheses.

### Package Information

<table>
<thead>
<tr>
<th>Package</th>
<th>Area</th>
<th>IO MGT</th>
<th>Notes</th>
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<td>220</td>
<td>21.8</td>
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### Hard IP Resources

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### Embedded Hard IP Resources

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