

		Virtex-5 LX Platform Optimized for High-performance Logic (1.0 Volt)							Virtex-5 LXT Platform Optimized for High-performance Logic with Low-power Serial Connectivity (1.0 Volt)								Virtex-5 SXT Platform Optimized for DSP with Low-power Serial Connectivity (1.0 Volt)		
Part Number		XC5VLX30	XC5VLX50	XC5VLX85	XC5VLX110	XC5VLX155	XC5VLX220	XC5VLX330	XC5VLX20T	XC5VLX30T	XC5VLX50T	XC5VLX85T	XC5VLX110T	XC5VLX155T	XC5VLX220T	XC5VLX330T	XC5VSX35T	XC5VSX50T	XC5VSX95T
EasyPath™ Cost Reduction Solutions ⁽¹⁾		—	—	XCE5VLX85	XCE5VLX110	XCE5VLX155	XCE5VLX220	XCE5VLX330	XCEVLXT20T	—	—	XCEVLXT85T	XCE5VLX110T	XCE5VLX155T	XCE5VLX220T	XCE5VLX330T	—	XCE5VSX50T	XCE5VSX95T
Logic Resources	Slices ⁽²⁾	4,800	7,200	12,960	17,280	24,320	34,560	51,840	3,120	4,800	7,200	12,960	17,280	24,320	34,560	51,840	5,440	8,160	14,720
	Logic Cells ⁽³⁾	30,720	46,080	82,944	110,592	155,648	221,184	331,776	19,968	30,720	46,080	82,944	110,592	155,648	221,184	331,776	34,816	52,224	94,208
	CLB Flip-Flops	19,200	28,800	51,840	69,120	97,280	138,240	207,360	12,480	19,200	28,800	51,840	69,120	97,280	138,240	207,360	21,760	32,640	58,880
Memory Resources	Maximum Distributed RAM (Kbits)	320	480	840	1,120	1,640	2,280	3,420	210	320	480	840	1,120	1,640	2,280	3,420	520	780	1,520
	Block RAM/FIFO w/ECC (36Kbits each)	32	48	96	128	192	192	288	26	36	60	108	148	212	212	324	84	132	244
	Total Block RAM (Kbits)	1,152	1,728	3,456	4,608	6,912	6,912	10,368	936	1,296	2,160	3,888	5,328	7,632	7,632	11,664	3,024	4,752	8,784
Clock Resources	Digital Clock Managers (DCM)	4	12	12	12	12	12	12	2	4	12	12	12	12	12	12	4	12	12
	Phase Locked Loop (PLL)/PMCD	2	6	6	6	6	6	6	1	2	6	6	6	6	6	6	2	6	6
I/O Resources ⁽⁴⁾	Maximum Single-Ended I/Os	400	560	560	800	800	800	1,200	160	360	480	480	680	680	680	960	360	480	640
	Maximum Differential I/O Pairs	200	280	280	400	400	400	600	80	180	240	240	340	340	340	480	180	240	320
	I/O Standards	HT, LVDS, LVDSSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II																	
Embedded Hard IP Resources ⁽⁵⁾	DSP48E Slices	32	48	48	64	128	128	192	24	32	48	48	64	128	128	192	192	288	640
	PCI Express Endpoint Blocks	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	10/100/1000 Ethernet MAC Blocks	0	0	0	0	0	0	0	2	4	4	4	4	4	4	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers	0	0	0	0	0	0	0	4	8	12	12	16	16	16	24	8	12	16
Speed Grades	Commercial	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2
Configuration	Configuration Memory (Mbits)	8.4	12.6	21.8	29.1	42.7	53.1	79.7	6.5	9.4	14.1	23.3	31.1	43.0	55.1	82.7	13.3	20.0	35.7
Package ^(6,7)		Area		Available User I/Os															
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)																			
FF324	19 x 19 mm	220	220																
FF676	27 x 27 mm	400	440	440	440														
FF1153	35 x 35 mm		560	560	800	800													
FF1760	42.5 x 42.5 mm				800	800	800	1200											
FF323	19 x 19mm								172 (4)	172 (4)									
FF665	27 x 27mm									360 (8)	360 (8)						360 (8)	360 (8)	
FF1136	35 x 35mm										480 (12)	480 (12)	640 (16)	640 (16)				480 (12)	640 (16)
FF1738	42.5 x 42.5mm												680 (16)	680 (16)	680 (16)	960 (24)			

- Notes:
- EasyPath™ solutions provide a conversion-free path for volume production.
 - A single Virtex-5 CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
 - Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
 - Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 - One system monitor block included in all devices.
 - Available I/O for each device-package combination: number of SelectIO pins (number of RocketIO transceivers).
 - All products available Pb-free and RoHS-Compliant.