

## Education Services



### The Fastest Course to Success

Effective January 1st, 2007

# Design Smaller, Faster, Cheaper...

Xilinx Education Services delivers everything you need to get your designs completed on time, on budget and with optimal performance.

Xilinx Education Services can help you reduce costs by:

- Designing into a smaller FPGA
- Targeting a slower Speed Grade FPGA
- Reducing your learning curve to meet your time-to-market window

With public, private, and online training available worldwide you can be sure to find a training offering that best fits your needs.

## FPGA DESIGN

### Fundamentals of FPGA Design

Level: Fundamental

Duration: 1 day

Understand Xilinx FPGA architecture and learn to implement a complete design in one day. This course provides you with an introduction to designing with Xilinx FPGAs using Xilinx ISE™ software. Features covered in this course include the Architecture Wizard, pin assignments, and creating area constraints (PACE). Other topics include design planning, implementation options, and global timing constraints. Reduce your learning curve through several practical labs.

### Design Techniques for Lower Cost

Level: Fundamental

Duration: 1 day

This workshop will appeal to engineers who have an interest in developing low-cost products, particularly in high-volume markets. The workshop covers several different design techniques — such as estimating design size, applying design techniques, and exploring creative ways to use FPGA memory resources — all in an effort to reduce design costs. This course features the Spartan™ family of devices.

### TMRTool

Level: Fundamental to Intermediate

Duration: 2 days

This comprehensive course is a thorough introduction to the Xilinx TMR (XTMR) solution for designs that require Triple Module Redundancy. The XTMR solution incorporates TMRTool, a proprietary software application that offers total control and flexibility for the TMR process for Xilinx FPGAs.

### Designing for Performance

Level: Intermediate

Duration: 2 days

Learn techniques to help improve your design's performance. This course builds on the principles covered in our Fundamentals of FPGA Design course with an emphasis on achieving timing closure. Topics include FPGA design techniques, HDL coding techniques, the CORE Generator™ system, power estimation, timing analysis, advanced timing constraints, and advanced implementation options. This course is also offered periodically live online.

### Designing with the Virtex-4 Family

Level: Intermediate

Duration: 2 days

Interested in learning how to effectively utilize Virtex™-4 architectural resources? Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance, this course focuses on understanding, as well as designing into, several of the new and enhanced resources found in our newest device. Features covered include a Virtex-4 FPGA overview, DCM and PMCD, global and regional clocking techniques, memory and FIFO, and source-synchronous resources. A combination of modules and labs allows for practical hands-on application of the principles taught.

### Designing with the Virtex-5 LX and LXT Platform FPGA

Level: Intermediate

Duration: 1 day

Interested in learning how to effectively utilize Virtex™-5 FPGA architectural resources? Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device.

### Designing with PlanAhead

Level: Intermediate

Duration: 2 days

Learn to increase design performance and achieve repeatable performance by using the PlanAhead™ software tool. Topics include: Product Overview, Synthesis and Project Tips, Design Analysis, Creating a Floorplan, Improving Performance, Incremental Methodology, and Block-Based IP Design.

### Advanced FPGA Implementation

Level: Advanced

Duration: 2 days

Push the limits of your design by learning techniques that will increase your overall proficiency. This course builds on the principles covered in our Fundamentals of FPGA Design and Designing for Performance courses. Some of the concepts that you will learn include incremental and modular design techniques, creating floorplans, using scripting, implementing relationally placed macros, editing and simplifying constraints files, using FPGA Editor for advanced implementation editing, and using clock resources effectively.

## CPLD DESIGN

### Fundamentals of CPLD Design

Level: Fundamental

Duration: 1 day

An introduction to designing with Xilinx CPLDs using ISE Software. This course will take a student from an introduction to programmable logic, to optimizing designs, to taking full advantage of the architectural features of CoolRunner-II™ CPLDs.

### Designing for Performance for CPLDs

Level: Intermediate

Duration: 1 day

This course is a comprehensive overview on CPLD software flow. By applying the techniques presented in the course, you will be able to enhance design performance and to make the best possible use of Xilinx CPLD architectures.

## DSP DESIGN

### DSP Design Using AccelDSP Synthesis Tools

Level: Beginner

Duration: 2 days

Learn how to synthesize an algorithm written in MATLAB into a design that is optimized for a Xilinx FPGA. Learn how to make MATLAB coding changes that improve area and performance. Use the floating- to fixed-point and design exploration features of the AccelDSP Synthesis Tool to achieve maximum results. Learn how to merge a synthesized MATLAB block into a larger HDL design or System Generator design.

### DSP Design Using System Generator

Level: Intermediate

Duration: 2 days

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware-in-the-loop verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

### DSP Implementation Techniques for Xilinx FPGAs

Level: Advanced

Duration: 3 days

This course bridges the gap between the DSP algorithm/system designer and the hardware engineer. While describing how algorithms can be efficiently implemented, the course techniques also demonstrate which decisions, at the system level, have the greatest impact on the implementation process, resource costs, and performance.

## EMBEDDED SYSTEMS DESIGN

### Embedded Systems Development

Level: Intermediate

Duration: 2 days

Looking for a hands-on approach to developing embedded systems? Attend this training to gain a better understanding of developing a PowerPC™ and MicroBlaze™ embedded system by using the Embedded Development Kit (EDK). This course will provide hands-on labs regarding the development, debug, and simulation of the embedded system. Labs provide users with a choice of targeting either PowerPC or MicroBlaze systems.

### Advanced Features and Techniques of Embedded Systems Development

Level: Advanced

Duration: 2 days

Understand and utilize advanced components of embedded systems design in order to architect a complex system. This course builds on the skills learned in the Embedded Systems Development course. Topics include external memory interfacing using various memory interface cores; enhancing performance through profiling, caching, and dedicated links; hardware and software debugging using the Xilinx software debugger and ChipScope Pro; bus functional models and simulation; interrupts, setting counter timer facilities and the PPC core clock; OCM; board support package using Xilinx lightweight kernel and Linux; and debugging techniques. The majority of this course is spent on practical hands-on lab work such as external memory interfacing, hardware and software debugging using ChipScope Pro, bootloader, simulation using bus functional model, and profiling.

## CONNECTIVITY DESIGN

### Designing with Multi-Gigabit Serial I/O

Level: Intermediate

Duration: 2 days

Learn how to employ RocketIO™ in your Virtex-II Pro design. Understand and utilize the features of the RocketIO transceiver blocks, such as CRC, 8b/10b encoding, channel bonding, clock correction, and comma detection. Additional highlighted topics include debugging techniques, use of the Architecture Wizard, synthesis and implementation considerations, and standards compliance. This comprehensive course equally balances lecture modules with practical hands-on lab work.

### Signal Integrity for High-Speed Memory and Processor I/O

Level: Intermediate

Duration: 2 days

Learn how signal integrity techniques are applicable to high-speed interfaces between Xilinx FPGAs and semiconductor memories. This course teaches you about high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS models and complete simulations using CAD packages. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules and practical hands-on labs.

### Designing a LogiCORE™ PCI System

Level: Intermediate

Duration: 2 days

Learn the tips and tricks of PCI design in this two-day course, which provides an introduction to basic PCI concepts and architecture as well as intensive training on designing with the PCI core for Xilinx. This course emphasizes and illustrates how PCI transactions take place, and gives you an overview of Xilinx PCI solutions. You will learn the basics of Xilinx PCI cores including PCI 64/66 and PCI 32. You will also learn design concepts and basic verification strategies for creating a PCI system design. The labs cover the basic transaction analysis using the ModelSim® simulator and the general design flow, from core to verification using ISE.

### Designing a LogiCORE PCI-X System

Level: Intermediate

Duration: 2 days

This course focuses on the PCI-X 2.0 specification and provides a detailed investigation into the operation of the PCI-X LogiCORE. The emphasis is on how PCI-X transactions take place, including a brief review of PCI protocol fundamentals. Explaining the principles and concepts introduced by the PCI-X Addendum, this course also provides an in-depth understanding of the PCI-X LogiCORE and how a digital designer may interface this to a typical user application to create a flexible PCI-X solution.

### Designing a LogiCORE PCI Express System

Level: Intermediate

Duration: 2 days

By learning PCI Express core protocol fundamentals, designers can gain a working knowledge of how PCI Express can be used in their systems. This course focuses on the PCI Express protocol subjects that designers, using the Xilinx PCI Express core should understand to complete their designs faster and easier. Students will also be introduced to each Xilinx PCI Express core product and will gain intimate knowledge of how the PCI Express core operates.

### Designing with Ethernet MAC Controllers

Level: Intermediate

Duration: 2 days

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements.

## LANGUAGES

### Introduction to Verilog

Level: Fundamental

Duration: 3 days

This comprehensive course is an effective introduction to the Verilog language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design by using a top-down synthesis approach. This course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

### Introduction to VHDL

Level: Fundamental

Duration: 3 days

This comprehensive course is an effective introduction to the VHDL language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design by using a top-down synthesis design approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

### Advanced VHDL

Level: Advanced

Duration: 2 days

Increase your VHDL proficiency by learning advanced techniques to help you write more robust and reusable code. This comprehensive course is targeted towards designers who already have some experience with VHDL. The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs, as compared to lecture modules.

## XILINX WORLDWIDE EDUCATION SERVICES

Xilinx education courses are offered by Authorized Training Providers (ATPs) in most regions of the world, providing you expert training opportunities. Customer courses offered by our ATPs use high-quality training materials developed by Xilinx, and leverage the specialized knowledge and extensive network of our ATPs. **Pricing and availability of classes varies by region.**

Authorized Training Provider	Contact	Country/Region(s) Supported
Xilinx Education Services	<a href="http://www.xilinx.com/education">www.xilinx.com/education</a>	Worldwide
<b>North America</b>		
Technically Speaking Inc.	<a href="http://www.technically-speaking.com">www.technically-speaking.com</a>	Arizona, Southern California, New Mexico, Nevada Others
Xilinx Education Services	<a href="http://www.xilinx.com/education">www.xilinx.com/education</a>	
<b>Europe/Americas</b>		
Arcobel Embedded Solutions Doulos Ltd F'SATIE Inline Group Logtel Computer Communications (1984), Ltd. Magnetic Digital Systems Mindway Multi Video Designs (MVD)	<a href="http://www.arcobel.nl">www.arcobel.nl</a> <a href="http://www.doulos.com/xilinx/training@fsatie.ac.za">www.doulos.com/xilinx/training@fsatie.ac.za</a> <a href="mailto:yuliy@inlinegroup.ru">yuliy@inlinegroup.ru</a> <a href="mailto:asherrubin@logtel.com">asherrubin@logtel.com</a> <a href="mailto:education@magneticgroup.ru">education@magneticgroup.ru</a> <a href="mailto:valerio.scibilia@mindwaydesign.com">valerio.scibilia@mindwaydesign.com</a> <a href="http://www.mvd-fpga.com">www.mvd-fpga.com</a>	The Netherlands, Belgium, Luxemburg United Kingdom, Ireland South Africa, Zimbabwe, Botswana Moscow Region Israel, Turkey Urals Region Italy France, Spain, Portugal, Switzerland, Mexico Brazil, Argentina Ukraine
Pulsar Ltd Programmable Logic Competence Center (PLC2)	<a href="mailto:vict.pulsar@a-teleport.com">vict.pulsar@a-teleport.com</a> <a href="http://www.plc2.de">www.plc2.de</a>	Germany, Switzerland, Poland, Hungary, Czech Republic, Slovakia, Slovenia, Greece, Cyprus, Turkey, Russia Austria, Czech Republic, Hungary, Slovakia, Slovenia Sweden, Norway, Denmark, Finland, Lithuania, Latvia, Estonia
SO-Logic Consulting	<a href="http://www.so-logic.co.at">www.so-logic.co.at</a>	
Bitsim AB	<a href="mailto:info@fpgatraining.com">info@fpgatraining.com</a>	
<b>Asia Pacific</b>		
Activemedia Innovation Pte Ltd Black Box Consulting ENGSoft Korea Inc. E-elements Co., Ltd OE-Galaxy, Co. Ltd. Sandeevani Programmable Solutions Pvt. Ltd. Symmid Corporation Sdn Bhd Ulinx Corporation	<a href="http://www.activemedia.com.sg/">www.activemedia.com.sg/</a> <a href="http://www.blackboxconsulting.com.au">www.blackboxconsulting.com.au</a> <a href="http://www.engsoftkorea.com">www.engsoftkorea.com</a> <a href="http://www.e-elements.com">www.e-elements.com</a> <a href="http://www.oegalaxy.com.vn">www.oegalaxy.com.vn</a> <a href="http://www.sandeevani-vlsi.com">www.sandeevani-vlsi.com</a> <a href="http://www.symmid.com">www.symmid.com</a> <a href="http://www.ulinx.com.tw">www.ulinx.com.tw</a>	Singapore, Thailand Australia, New Zealand Korea China, Hong Kong Vietnam India Malaysia Taiwan
<b>Japan</b>		
Agilent Technologies Japan, Ltd. Avnet Japan Paltek Ryoyo Electro Corporation Shinko Shoji Co., Ltd. Tokyo Electron Device Ltd.	<a href="http://www.agilent.co.jp">www.agilent.co.jp</a> <a href="http://www.jp.avnet.com">www.jp.avnet.com</a> <a href="http://www.paltek.co.jp">www.paltek.co.jp</a> <a href="http://www.ryoyo.co.jp">www.ryoyo.co.jp</a> <a href="http://xilinx.shinko-sj.co.jp">xilinx.shinko-sj.co.jp</a> <a href="http://ppg.teldevice.co.jp">ppg.teldevice.co.jp</a>	Japan Japan Japan Japan Japan Japan

## ADDITIONAL EDUCATION SERVICES

**Curriculum Paths** — Curriculum paths illustrate the recommended course sequence to follow based on your design specialization. Because Xilinx courses build on each other, you must meet the prerequisites to gain the full benefit of each course. Prerequisites are outlined in the course descriptions.  
[http://www.xilinx.com/support/training/cur\\_paths/atp-index.htm](http://www.xilinx.com/support/training/cur_paths/atp-index.htm)

**Skills Assessments** — Not sure if a particular course is appropriate for you? Take our online Skills Assessment to evaluate your knowledge and competency with respect to one of Xilinx Education Services classes.  
<http://www.xilinx.com/support/training/skills-assessment-faq.htm>

**Recorded e-Learning** — Recorded e-Learnings are currently available at no charge, over the Internet anytime, day or night, worldwide to allow you to get up to speed quickly. New topics each month, such as: Clocking Techniques, Timing Closure, DDR Memory Interface, FPGA vs. ASIC, etc.  
<http://www.xilinx.com/support/training/free-courses.htm>

**Live e-Learning (North America only)** — A handful of the instructor-led courses listed are delivered as Live e-Learning as well. Course modules are scheduled sequentially over a 1 to 3 week period, depending upon the subject. View schedules online. <http://www.xilinx.com/support/training/na-atp.htm>

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