



DESIGN FOR THE NEXT DECADE  
OF 'ALL PROGRAMMABLE' DEVICES

### ➤ Xilinx Solution Highlights

- Next generation of system-to-IC level tools, built on the backbone of a shared scalable data model and a common debug environment
- 4x productivity advantage drives beyond programmable logic to programmable systems integration
- 'All Programmable' device support including 3D stacked silicon interconnect technology, ARM processing systems and Analog Mixed Signal (AMS)

### IP AND SYSTEM-CENTRIC TOOL SUITE ACCELERATING PROGRAMMABLE SYSTEMS INTEGRATION AND IMPLEMENTATION BY UP TO 4X

Programmable devices are at the heart of most systems today, enabling not only programmable logic design, but programmable systems integration. Xilinx has transformed from an FPGA company to an 'All Programmable' company, offering technology from logic and IO to SW programmable ARM® processing systems and beyond.

With the next decade of programmable platforms, comes the next generation design environment that meets the aggressive pace and the need for enhanced productivity. Xilinx introduces the Vivado™ Design Suite, an IP and system-centric design environment built from the ground up to accelerate productivity for the next generation of 'All Programmable' devices. The new Vivado Design Suite is already proven to accelerate integration and implementation by 4x over traditional design flows, reducing cost by simplifying design and automating, not dictating, a flexible design environment.

Vivado Design Suite provides a highly integrated design environment with a completely new generation of system-to-IC level tools, all built on the backbone of a shared scalable data model and a common debug environment. It is also an open environment based on industry standards such as AMBA® AXI4 interconnect, IP-XACT IP packaging metadata, the Tool Command Language (Tcl), Synopsys® Design Constraints (SDC) and others that facilitates customized design flows. Vivado was architected to enable the combination of all types of programmable technologies and scale up to 100M ASIC equivalent gate designs.

## Accelerating Integration and Implementation

To eliminate bottlenecks in integration, the Vivado Design Suite includes electronic system level (ESL) design for rapidly synthesizing and verifying C/C++/SystemC-based algorithmic IP, standards based packaging of both algorithmic and RTL IP for reuse, standards based IP stitching and systems integration of all types of IP, and the verification of blocks and systems with 3X faster simulation and HW Co-simulation provides 100X performance.

The Vivado Design Suite accelerates the implementation process by enabling more turns per day and helping to eliminate them altogether. The new Vivado data model improves run times up to 4x compared to competing solutions. Vivado includes a hierarchical chip planner, a 3-15X faster logic synthesis tool with industry leading support for SystemVerilog, and a 4X faster, more deterministic place and route engine that uses analytics to minimize a 'cost' function of multiple variables such as timing, wire length and routing congestion. In addition, incremental flows allow for ECO (Engineering Change Order) induced changes to be quickly processed by only re-implementing a small part of the design, while preserving performance. Finally, leveraging the new shared scalable data model, power, timing and area estimates are provided at every stage of the design flow, enabling up front analysis and then optimization with integrated capabilities such as automated clock gating.

## VIVADO DESIGN SUITE EDITIONS

PILLARS OF PRODUCTIVITY	FEATURES	WEBPACK (DEVICE LIMITED)	DESIGN EDITION	SYSTEM EDITION
IP Integration and Implementation	Integrated Design Environment	●	●	●
	Software Development Kit (SDK)	●	●	●
Verification and Debug	Vivado Simulator	Limited	●	●
	Vivado Logic Analyzer		●	●
	Vivado Serial I/O Analyzer		●	●
Design Exploration and IP Generation	Vivado High-Level Synthesis			●
	System Generator for DSP			●

## Take the NEXT STEP

For more information about Vivado Design Suite and availability, please visit: [www.xilinx.com/vivado](http://www.xilinx.com/vivado)

### Corporate Headquarters

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
USA  
Tel: 408-559-7778  
[www.xilinx.com](http://www.xilinx.com)

### Europe

Xilinx Europe  
One Logic Drive  
Citywest Business Campus  
Saggart, County Dublin  
Ireland  
Tel: +353-1-464-0311  
[www.xilinx.com](http://www.xilinx.com)

### Japan

Xilinx K.K.  
Art Village Osaki Central Tower 4F  
1-2-2 Osaki, Shinagawa-ku  
Tokyo 141-0032 Japan  
Tel: +81-3-6744-7777  
[japan.xilinx.com](http://japan.xilinx.com)

### Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific  
5 Changi Business Park  
Singapore 486040  
Tel: +65-6407-3000  
[www.xilinx.com](http://www.xilinx.com)



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