## Zynq-7000 All Programmable SoCs

### Zynq-7000 All Programmable SoC

#### Device Name
- Z-7010
- Z-7020
- Z-7030
- Z-7065
- Z-7070
- Z-7100

#### Part Number
- XC7Z010
- XC7Z020
- XC7Z030
- XC7Z065
- XC7Z070
- XC7Z100

### Processing System

#### Processor Extensions
- Dual ARM® Cortex™-A9 MPCore™ with CoreSight™ NEON™ & Single / Double Precision Floating Point for each processor

#### Maximum Frequency
- 868 MHz
- 32 KB Instruction, 32 KB Data per processor
- Up to 1 GHz (1)

#### L1 Cache
- 1 L1 Cache
- 2 L2 Cache

#### On-Chip Memory
- DDR1
- DDR3

#### Peripheral Support (2)
- 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO

#### DMA Channels
- RCA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot

#### Security (3)
- AES and SHA 256b ADs with up to 17 Differential Inputs

#### External Memory Support (2)
- DDR1, DDR3, DDR2, LPDDR2

#### Ping/Pong
- 2x UART
- 2x CAN 2.0B, 2x ODC, 2x SPI, 4x 32b GPIO

#### External Static Memory Support (2)
- 2x Dual SPI, NAND, NOR

#### Programmable Logic

#### Xilinx 7 Series Programmable Logic Equivalent
- 2,622 GMACs
- Gen2 x8

#### Artix-7 FPGA
- 17,800
- 46,200
- 53,200

#### Artix-7 FPGA
- 512 KB
- 819 KB
- 1.33 MB

#### Artix-7 FPGA
- 32 KB
- 65 KB
- 125 KB

#### Artix-7 FPGA
- 166 MHz
- 200 MHz
- 270 MHz

#### Programmers
- 16 Interrupts
- 32 KB Instruction, 32 KB Data per processor

#### Maximum Transceiver Speed (Speed Grade Dependent)
- 6.6 Gb/s
- 12.5 Gb/s
- 10.3125 Gb/s

#### XMP087 (v1.10)
- Notes: 1. 1 GHz processor frequency is available only for -3 speedgrades for devices in flip-chip packages. Please see the data sheet for more details.

#### Summary
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Notes:
1. 1 GHz processor frequency is available only for -3 speedgrades for devices in flip-chip packages. Please see the data sheet for more details.
3. Security block is shared by the Processing System and the Programmable Logic.
4. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
5. Devices in the same package are footprint compatible. FBG70s and FG65s are also footprint compatible.
6. Static memory interfaces combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO Interface.
7. CLG45s and SBG45s are pin-to-pin compatible. See product data sheets and user guides for more details.

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