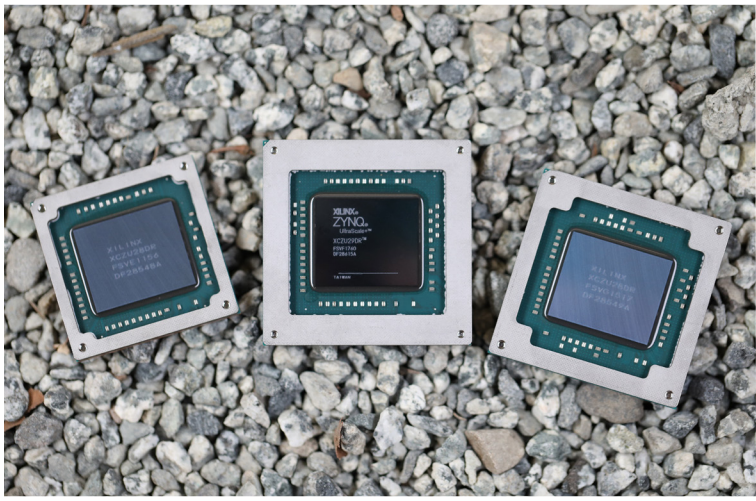
Zynq UltraScale+ RFSoC

- Integrated RF-Class Analog and Error Correction Technology
- Delivering 50-75% Power & Footprint Reduction
- Full Programmability across the RF Signal Chain



OVERVIEW

Zynq® UltraScale+™ RFSoCs integrate gigasample RF data converters and soft-decision forward error correction (SD-FEC) into an SoC architecture. The Zynq UltraScale+ RFSoC family simplifies system design with fewer components and provides platform hardware and software flexibility.

The portfolio features a breadth of devices with varying direct RF performance to meet diverse spectrum needs and use cases.

HIGHLIGHTS

Industry's Only Adaptable Single-Chip Radio Platform

- Integrated direct RF-sampling moves RF design to the digital domain
- User configurable SD-FEC integrated cores
- Programmable logic for diverse requirements and emerging standards
- Multicore heterogenous Arm®-based processing system
- Built on production-proven UltraScale™ architecture

Cost Effective and Power Efficient Devices

- Lower power by eliminating JESD204 interfaces
- Over 50% PCB area reduction vs. discrete solutions
- 80% more power efficient SD-FEC vs. a soft implementation

Future-Proof Comprehensive Solution

- Fulfilling 3G, 4G, and multiband 5G requirements
- Wide bandwidth for sub-6GHz and mmWave radio applications
- Fully integrated Remote-PHY solution for DOCSIS 3.1 standards
- L-Band, S-Band, and C-Band direct sampling

TARGET APPLICATIONS

- 4G and 5G Remote Wireless Infrastructure
- Remote Radio for Massive MIMO
- Fixed Wireless Access
- 5G Baseband
- Mobile Backhaul
- Phased Array Radar
- Remote-PHY for Cable Access DOCSIS 3.1
- Test and Measurement
- Satellite Communications
- Automotive LiDAR

FEATURES

	GEN 1	GEN 2	GEN 3
RF DATA CONVERTER SUBSYSTEM			
Maximum RF Input Frequency	4GHz	5GHz	6GHz
12-bit RF-ADCs	16x 2.058GSPS 8x 4.096GSPS	16x 2.275GSPS	-
14-bit RF-ADCs	-	-	8x 5.0GSPS 16x 2.5GSPS
14-bit RF-DACs	16x 6.554GSPS	16x 6.554GSPS	16x 10.0GSPS
User Configurable SD-FEC Blocks	8	0	8
LDPC Encode Throughput	19.8Gb/s	-	19.8Gb/s
LDPC Decode Throughput	2.84Gb/s @8 iterations	-	2.84Gb/s @8 iterations
Turbo Decode Throughput	1.78Gb/s @6 iterations	-	1.78Gb/s @6 iterations
PROGRAMMABLE LOGIC			
System Logic Cells (K)	930	930	930
DSP Slices	4,272	4,272	4,272
33G GTY Transceivers	16	16	16
Memory (Mb)	60.5	60.5	60.5
PCIe® Gen 3x16	2	2	-
PCIe Gen3 x16/Gen4 x8/CCIX	-	-	2
100G Ethernet Blocks with RS-FEC	2	2	2
150G Interlaken	1	1	1
PROCESSING SYSTEM			
Application Processor Core	Quad-core Arm Cortex®-A53 MPCore up to 1.33GHz		
Real-Time Processor Core	Dual-core Arm Cortex-R5 MPCore up to 533MHz		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4/3/3L; LPDDR4/3; External Quad-SPI; NAND; eMMC		

Note: All numbers are maximum capabilities

TAKE THE NEXT STEP

Zynq UltraScale+ RFSoCs are supported by comprehensive developments tools, reference designs, an IP catalog, and evaluation platforms.

For more information about Xilinx Zynq UltraScale+ RFSoCs, go to www.xilinx.com/rfsoc. Evaluation kits can be ordered separately. Visit Zynq UltraScale+ RFSoC Boards, Kits, and Modules for details and to place an order today.

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