



**XILINX**

**ALL PROGRAMMABLE™**

# **Xilinx 7 Series FPGA Power Benchmark Design Summary**

**May 2015**

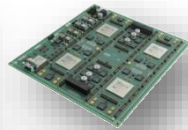
# Application-centric Benchmarking Process



100G Packet Processor



OTN Muxponder



ASIC Emulation



Wireless Radio & Satellite Modem



Edge QAM



AVB Switcher



Military Radio



Mobil Backhaul

FPGA resource counts, toggle rates, clock speeds...

➤ **Xilinx Power Estimator (XPE) version 2015.1**

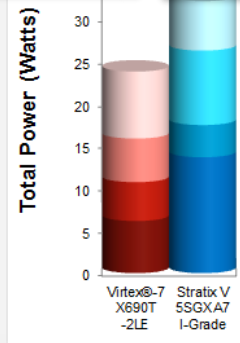
➤ **MAX condition used to estimate worst-case static power**

**XPE**

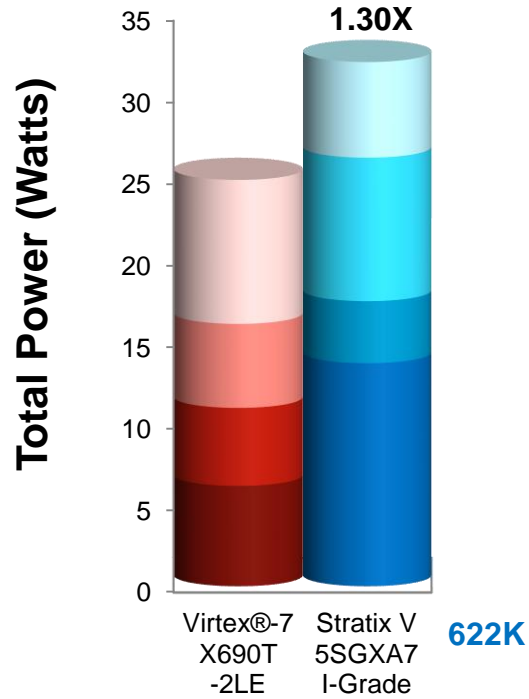
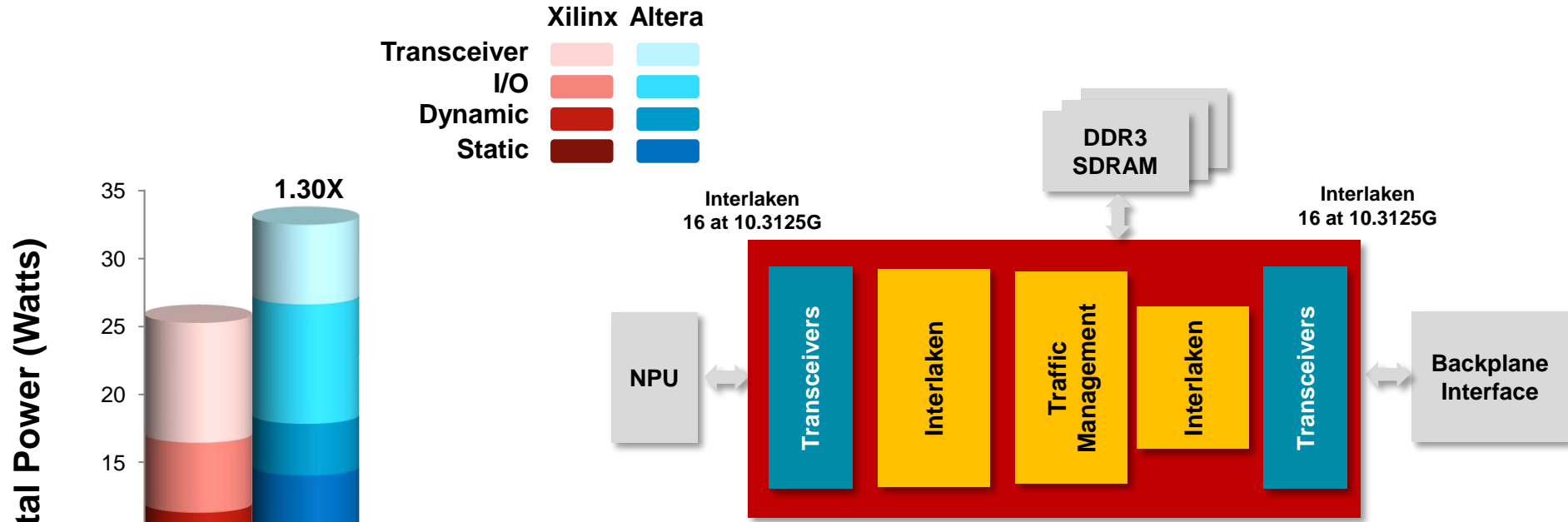
**Competitor's Estimator**

➤ **Early Power Estimator (EPE) versions 15.0**

➤ **MAX condition used to estimate worst-case static power**



# Power Benchmark: Traffic Manager in 100G Line Card Virtex-7 X690T FPGA



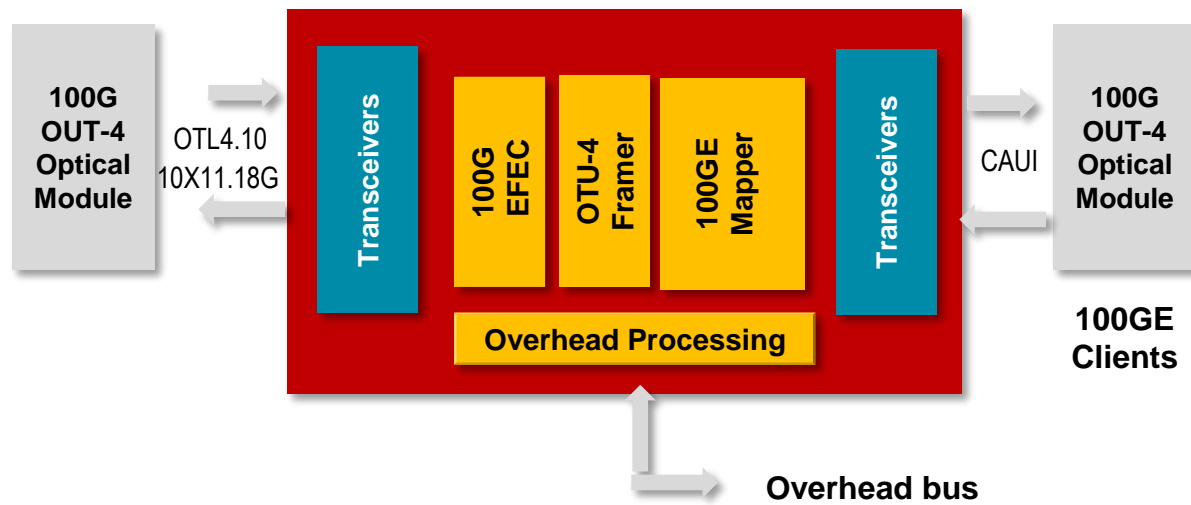
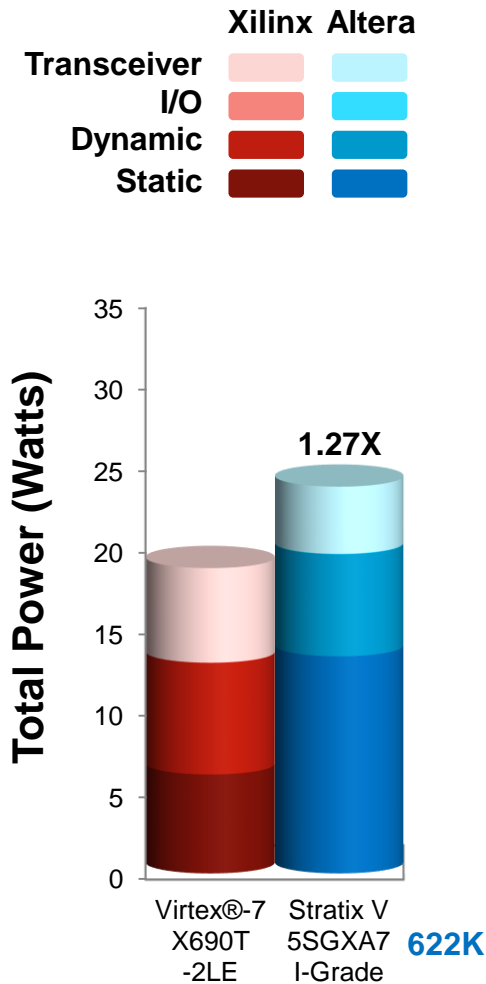
## Resources

Interface	I/Os	GTs	Rate
8 x 32-bit DDR3	544	-	1600 Mb/s
Interlaken	-	32	10.3 Gb/s

Environment	Process
Tj = 100°C	Max
<b>LC/LEs</b>	232K
<b>Flip-Flops</b>	167K
<b>Block RAM</b>	15,516 Kb
<b>DSP Blocks</b>	2
<b>PLLs</b>	8
<b>Core Freq.</b>	250 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Power Benchmark: 100GE over OTU4 Transponder Virtex-7 X690T FPGA



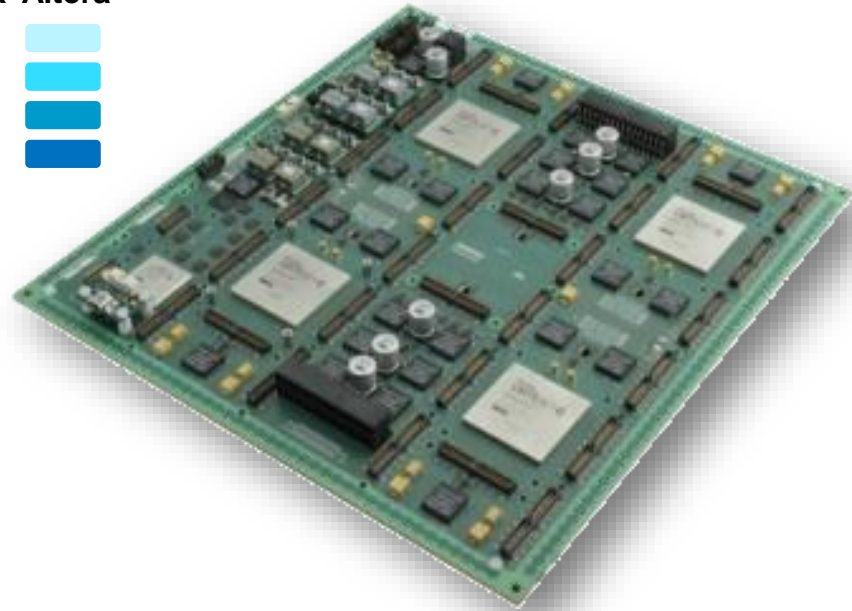
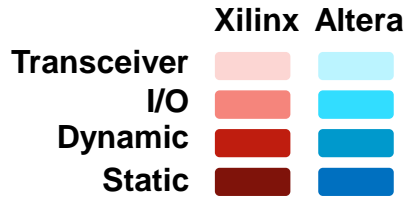
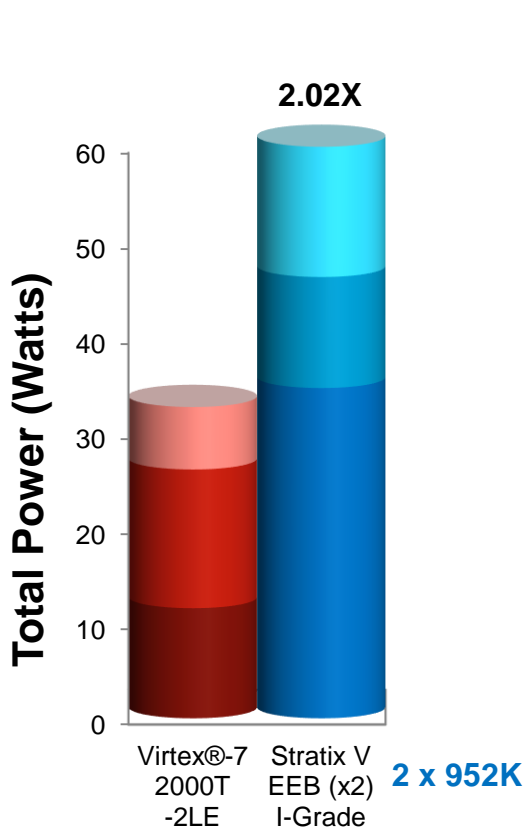
## Resources

Interface	I/Os	GTs	Rate
LVC MOS	50	-	250 Mb/s
GT	-	10	11.1 Gb/s
GT	-	10	10.3 Gb/s

Environment	Process
T <sub>j</sub> = 100°C	Max
<b>LC / LEs</b>	392K
<b>Flip-Flops</b>	245K
<b>Block RAM</b>	9,360 Kb
<b>Core Freq.</b>	350, 175 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Power Benchmark: ASIC Prototyping Virtex-7 FPGA 2000T



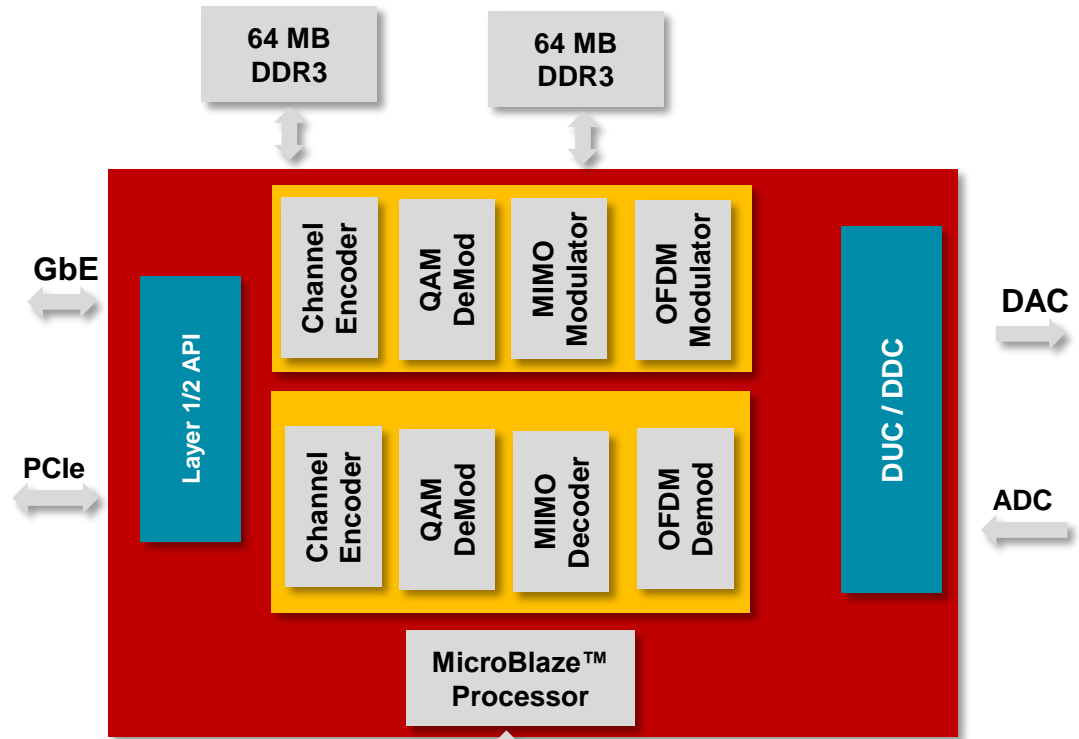
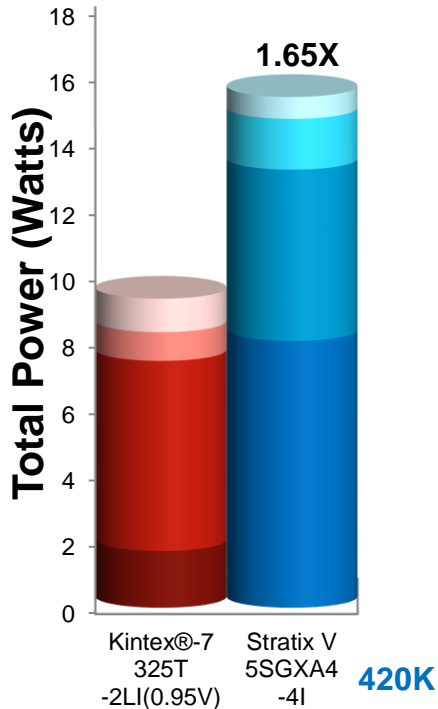
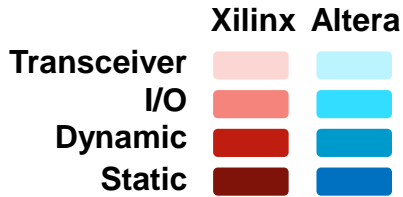
## Resources

Interface	I/Os	GTs	Rate
3 64-bit DDR3	366	-	1066 Mb/s
LVDS	408	-	1000 Mb/s

Environment	Process
T <sub>j</sub> = 100°C	Max
<b>LC / LEs</b>	1,224K
<b>Flip-Flops</b>	765 K
<b>Block RAM</b>	21,600 Kb
<b>Core Freq.</b>	200 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Power Benchmark: Wireless WCDMA / LTE Picocell Kintex-7 325T FPGA



## Resources

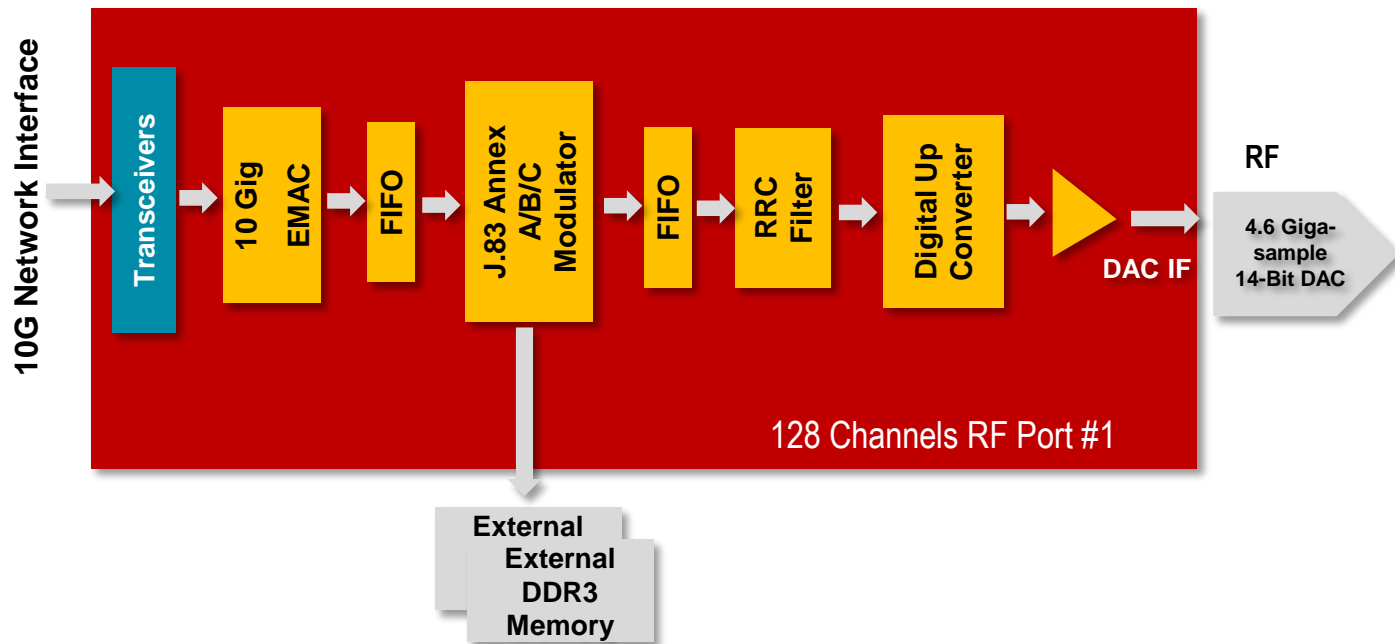
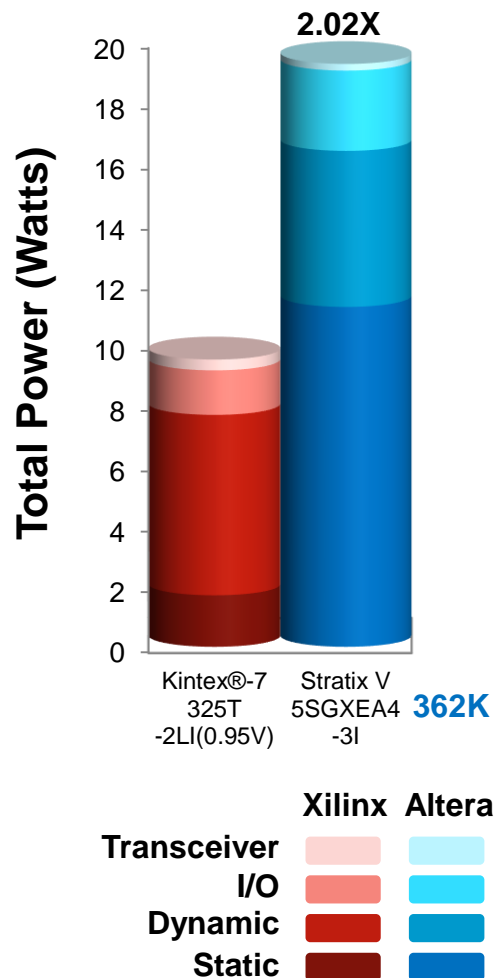
Interface	I/Os	GTs	Rate
3 x 16-bit DDR3	129	-	1066 Mb/s
GT	-	2	4.0 Gb/s
GT	-	1	1.25 Gb/s
GT	-	1	2.5 Gb/s

Environment	Process
Tj = 100°C	Max
<b>LC / LEs</b>	240K
<b>Flip-Flops</b>	150K
<b>Block RAM</b>	14,562 Kb
<b>DSP Blocks</b>	342
<b>PCIe® Blocks</b>	1
<b>Core Freq.</b>	307.2 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Dense Edge QAM Modulator

## Kintex-7 325T FPGA



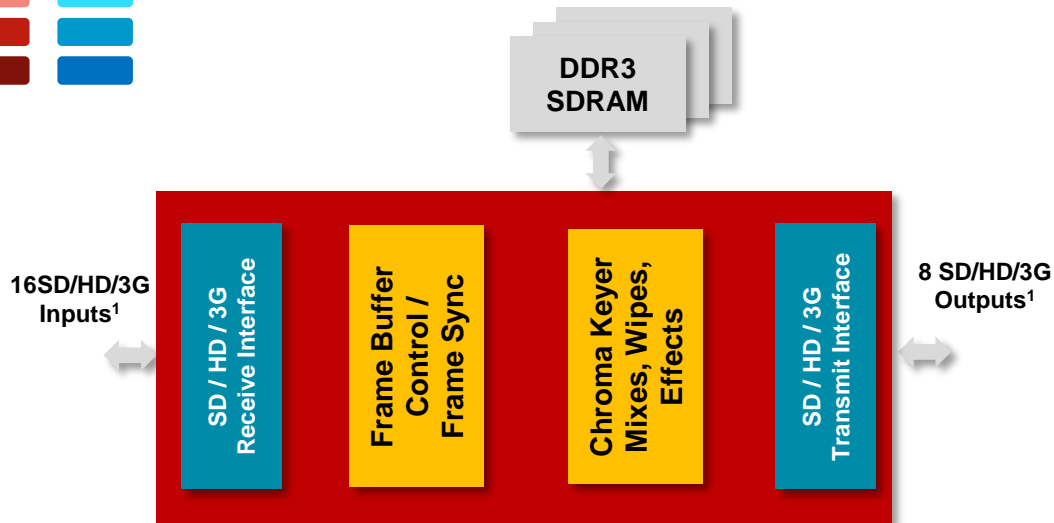
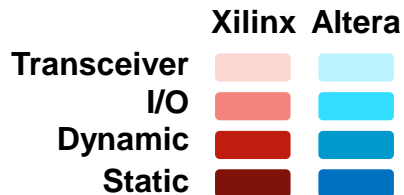
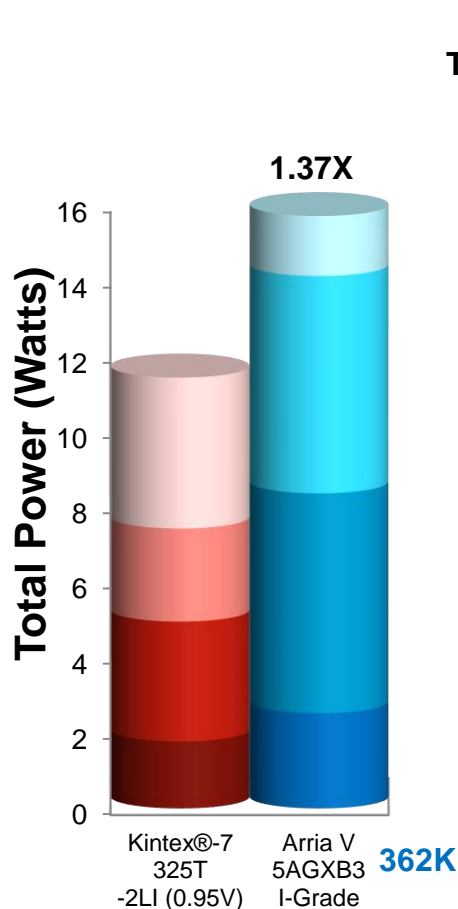
### Resources

Interface	I/Os	GTs	Rate
LVDS	124	-	1152 Mb/s
LVC MOS	12	-	15 MHz
2x 8-bit DDR3	55	-	800 Mb/s
GT	-	1	10.3 Gb/s

Environment	Process
T <sub>j</sub> = 100°C	Max
<b>LC / LEs</b>	182K
<b>Flip-Flops</b>	157K
<b>Block RAM</b>	12,402 Kb
<b>DSP Blocks</b>	641
<b>Core Freq.</b>	384, 576, 156, 192, 200 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Power Benchmark: AVB Switcher Kintex-7 325T FPGA



## Resources

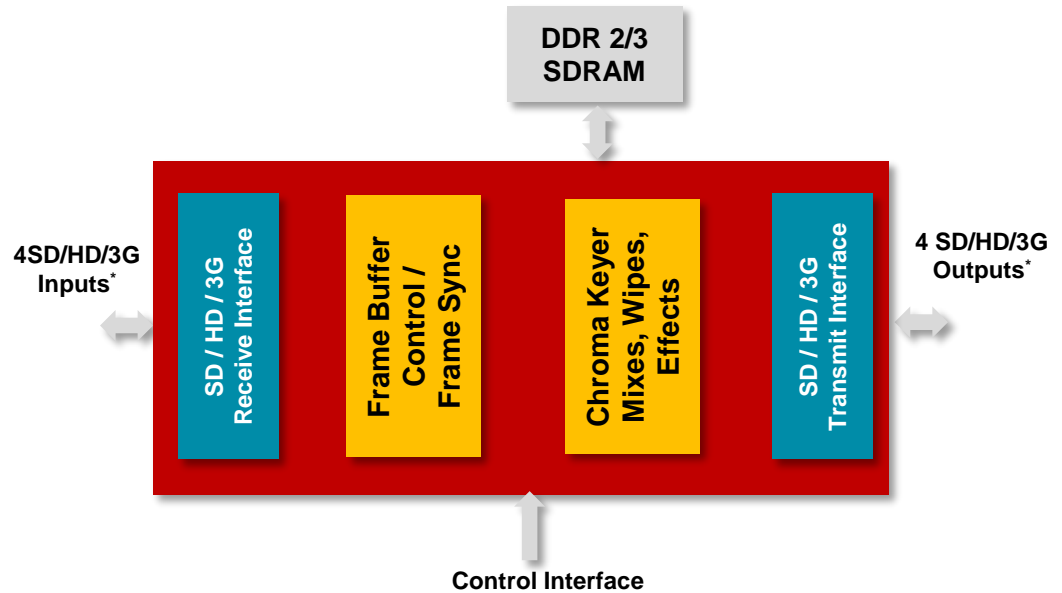
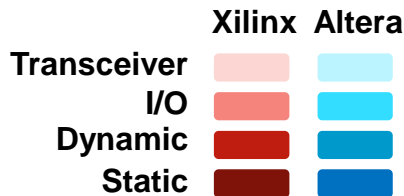
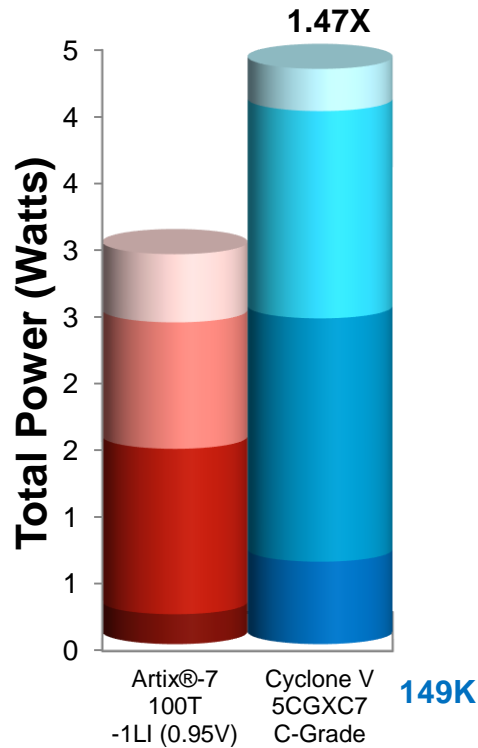
Interface	I/Os	GTs	Rate
3 x 72-bit DDR3	450	-	800 Mb/s
GT	-	16	2.97 Gb/s

Environment	Process
Tj = 100°C	Max
<b>LC / LEs</b>	300K
<b>Flip-Flops</b>	188K
<b>Block RAM</b>	10,800 Kb
<b>DSP Blocks</b>	500
<b>Core Freq.</b>	148.5 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0



# AVB Switcher (4-channel) Artix-7 100T FPGA



\*Note: SD/HD/3G inputs and outputs share GTs

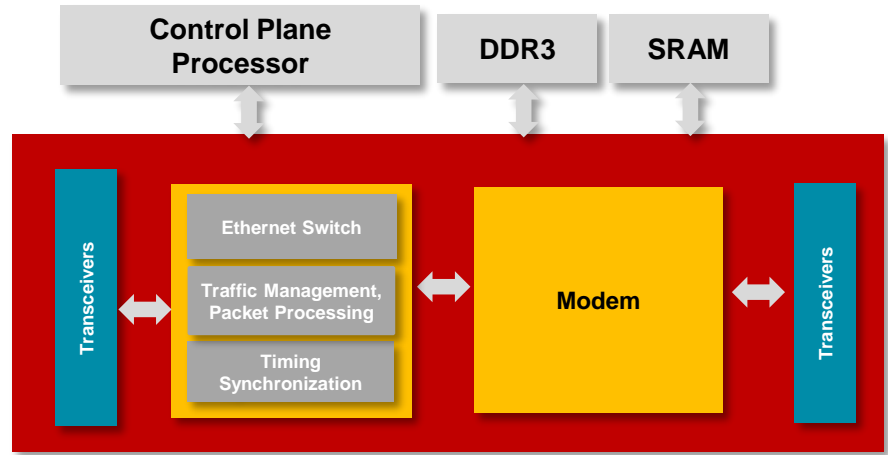
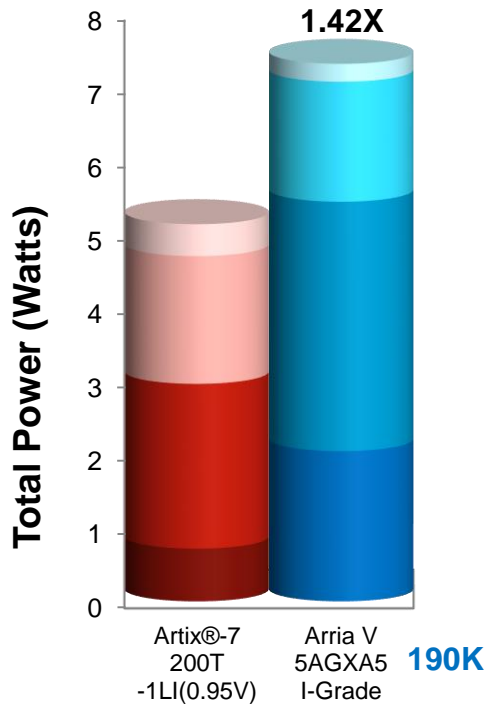
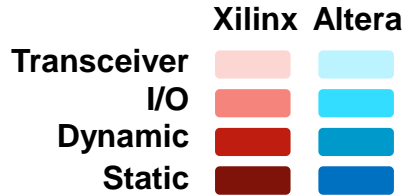
## Resources

Interface	I/Os	GTs	Rate
1 x 64-bit DDR3	112	-	800 Mb/s
GT	-	4	2.97 Gb/s

Environment	Process
Tj = 85°C	Max
<b>LC / LEs</b>	75K
<b>Flip-Flops</b>	47K
<b>Block RAM</b>	2,250 Kb
<b>DSP Blocks</b>	125
<b>PLL</b>	1
<b>Phaser Block</b>	1
<b>Core Freq.</b>	148.5, 400 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Power Benchmark: Single Channel Mobile Backhaul Artix-7 200T FPGA



## Resources

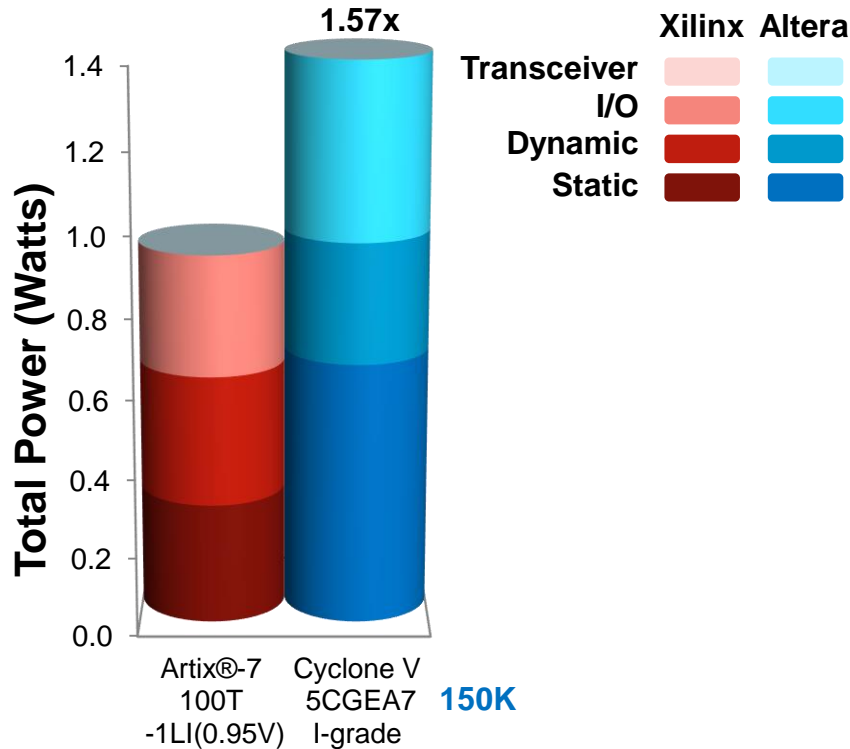
Interfaces	I/Os	GTs	Rate
1 x 32-bit DDR3	72	-	800 Mb/s
LVDS pairs	128	-	800 Mb/s
SEIO	150	-	100 Mb/s
Switch ports	-	4	1.0 Gb/s

Environment	Process
Tj = 100°C	Max
<b>LC / LEs</b>	130K
<b>Flip-Flops</b>	81K
<b>Block RAM</b>	5,076 Kb
<b>DSP Blocks</b>	345
<b>PLL</b>	2
<b>Core Freq.</b>	250, 400 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Power Benchmark: Satellite Modem

## Artix-7 100T FPGA



Environment	Process
T <sub>j</sub> = 85°C	Max
<b>LC/LEs</b>	85 K
<b>Flip-Flops</b>	52 K
<b>Block RAM</b>	3,420 Kb
<b>DSP Blocks</b>	126
<b>PLLs</b>	2
<b>Core Freq.</b>	30, 62.5, 125 MHz

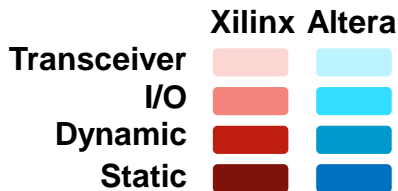
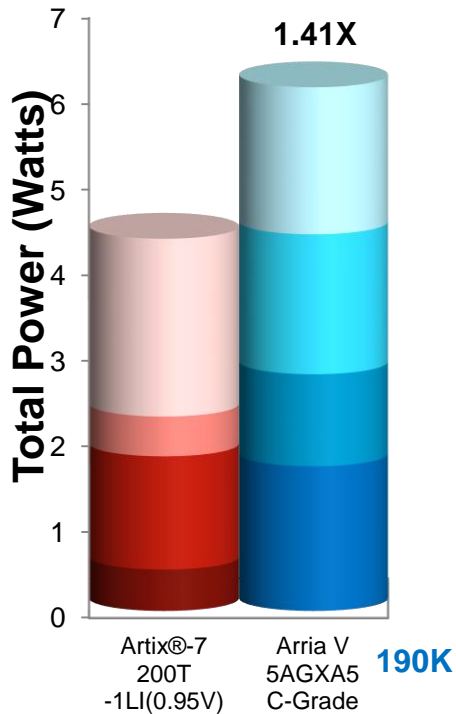
### Resources

Interface	I/Os	GTs	Rate
1x 32-bit DDR2	69	-	250 Mb/s

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0

# Military Network Protocol Platform Data Aggregator

## Artix-7 200T FPGA



### Resources

Interface	I/Os	GTs	Rate
2x 36-bit RLDRAMs	122	-	520 Mb/s
GT	-	6	5 Gb/s
GT	-	8	2.5 Gb/s
GT	-	1	2.5 Gb/s

Environment	Process
Tj = 85°C	Max
<b>LC / LEs</b>	63K
<b>Flip-Flops</b>	58K
<b>Block RAM</b>	3,600 Kb
<b>DSP Blocks</b>	400
<b>PCIe® Blocks</b>	1
<b>Core Freq.</b>	125 MHz

\*Design results sourced from Xilinx Power Estimator (XPE) version 2015.1 and Altera Early Power Estimator (EPE) version 15.0