

# Low-Cost EasyPath FPGAs Offer Promise to ASSP Companies

EasyPath FPGAs offer quick time to market and flexibility at prices below those offered by structured ASICs.

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As the semiconductor industry continues its march towards smaller process geometries, it has to deal with exponentially increasing mask set costs. Customers who want to spin a 90 nm ASIC must pay upwards of a million dollars in NRE. In addition, they must incur significant engineering and design expenses, increasing the overall cost of product development to prohibitive levels.

ASSP companies have come under increasing pressure to weigh more carefully the risk/reward tradeoffs for introducing new products. ASSP vendors are being forced to develop only those “blockbuster” products that will allow a reasonable return on their large up-front investments.

Recent innovations such as Xilinx® Spartan™-3 FPGAs and EasyPath™ technology, when used in combination with a wide IP portfolio, allow ASSP vendors to address many more opportunities in a cost-effective way while assuming minimal risks. In this article, we will examine how Spartan-3 FPGAs – together with their EasyPath counterparts – can alleviate some of the challenges faced by consumer electronics ASSP vendors.

## Customer-Specific FPGAs

Customer-specific FPGAs like those in the EasyPath program are identical to standard FPGA offerings, but use patented testing techniques to significantly improve yield. Once your design is frozen, Xilinx develops custom test patterns that specifically test only the resources used by that particular design. You reap the benefits of these consequently higher yields in the form of lower costs.

With EasyPath FPGAs, you can realize a 30-80% reduction in unit prices (compared to equivalent standard FPGAs) when you move to high volume. Because customer-specific FPGAs are the same piece of silicon as standard FPGAs – except cheaper – they offer a one-for-one match of all the features offered in a standard FPGA. As a result, almost no involvement is required from customer engineering teams; the conversion process from design completion to production is completely seamless.

Furthermore, the lead times from the time a design is frozen to volume production in customer-specific FPGAs can be as short as 8-10 weeks – an advantage of almost 12 weeks when compared to ASIC methodologies. Table 1 shows a comparison of EasyPath FPGAs versus structured ASIC methodologies, illustrating why EasyPath FPGAs are a better overall solution.

## Addressing ASSP Market Needs

Historically, ASSP vendors have used FPGAs as prototyping vehicles, moving to custom ASICs in high volume to take advantage of their low unit costs. This was a reasonable strategy at 0.18 $\mu$  and larger process nodes because lower NRE costs allowed companies to take the financial/market risk and go to market with multiple products.

As the demands of system integration, performance, and power have pushed ASSP vendors down to 0.13 $\mu$  and 90 nm, NRE costs and design complexity have increased significantly. A study in

Selection Criteria	Structured ASICs	EasyPath FPGAs
Time to Prototype Samples	4-8 Weeks	0 Weeks
Total Time to Volume Production	12-15 Weeks	8 Weeks
Vendor NRE/Mast Costs	\$100K-200K	\$75K
Design Cost for Conversion	\$250K-\$300K	\$0
Additional Cost of Tools for Conversion	\$100K-\$200K	\$0
Unit Costs	Low	Low
Risk	High	Low
Flexibility to Make Changes In-System	Inflexible	Flexible
Design Conversion from Prototype to Production	Additional Engineering	Conversion Free

\*Xilinx Market Analysis

Table 1 – EasyPath FPGAs offer significant advantages in time to market and total cost of ownership when compared to structured ASICs.

International Business Strategies' Fourth Quarter 2003 report estimates the product development cost of a 0.13 $\mu$  ASIC to be greater than \$10 million, including the cost of design, verification, and prototyping. This implies that an ASSP vendor has to sell at least 250,000 units of a \$40 ASP device (see Figure 1) just to recoup the development cost. Clearly, if other sales and marketing costs are included and a reasonable ROI is expected, the lifetime volume potential of a device must be significantly higher.

Customer-specific FPGAs, on the other hand, significantly reduce the mar-

ket/financial risk element. You can now have multiple variations of a particular design (or indeed, multiple designs) catering to different market segments – and go to market with all of them at the same time. This is because the NRE charges are minuscule compared to ASICs. You no longer need to spend valuable engineering resources to convert an FPGA design into an ASIC RTL, nor spend multiple weeks in verification and simulation to benefit from low-cost, high-volume solutions.

## Time to Market

In today's world of complex design cycles, short product life cycles, and quickly changing market needs, time to market is of paramount importance. Unfortunately, the complexity of deep sub-micron designs increases the time required to develop and debug a design, while increasing the risk of re-spins.

Because ASIC re-spins can set back a schedule at least three months, ASSP vendors take a tremendous risk of being late to market. Some studies have shown (as in the IBS 2003 report) that just a three-month slip in the schedule can cause a product revenue

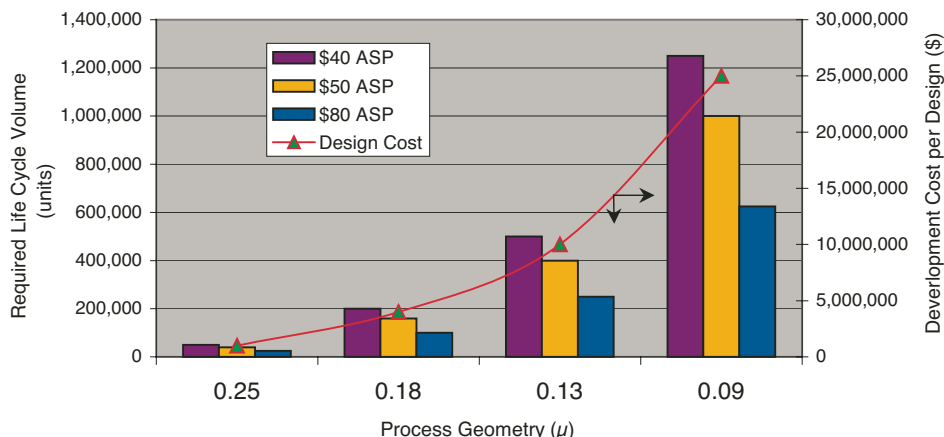


Figure 1 – The increasing cost of developing ASSPs as process nodes shrink means that companies are forced to go after high-volume “blockbuster” products to get a reasonable return on investment.

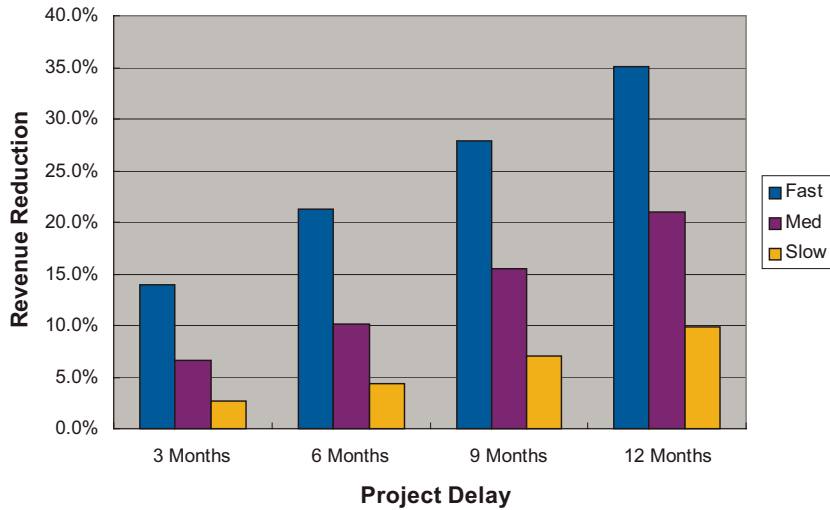


Figure 2 – The impact of time to market on product revenue in fast-, medium-, and slow-moving market segments (IBS 2003).

reduction of about 15% (see Figure 2). In the extreme case of seasonal products (widely prevalent in the consumer electronics industry), schedule slippage can mean that an ASIC product will miss customer demand altogether.

Customer-specific FPGAs allow ASSP vendors to postpone spending decisions until market uncertainties are removed. Once a design is completed, you no longer need to plan three to four months in advance and hope that the silicon you get at the end of the day works to your specifications. With one of the highest levels of reliability and shortest lead times in the industry, customer-specific FPGAs require ASSP vendors to incur little to no risk in the conversion process. Furthermore, with just eight to ten weeks to production, ASSP vendors can go to market with confidence and hit that prime market window.

### Technical Challenges

A common challenge that many ASSP vendors have to deal with is the changing landscape of industry standards. This is particularly true in wired telecom and wireless applications, where the lack of a coordinated effort to specify various telecommunications protocols and interface standards can result in incompatibilities between different vendors' products.

Ratifying standards is a time-consuming process and vendors often have to freeze their designs much earlier to get first-mover

advantages. ASSP vendors must either gamble that their final specifications will get adopted in a standard; implement a superset of all possible future combinations; or delay the design phase, running the risk of being late to market. These options are far from optimal.

One of the major advantages of FPGAs over ASICs is the flexibility to make design changes in case of a specification change or design error. Traditionally, designers have had to forgo this advantage as they move from FPGAs to an inflexible custom solution

like standard cell or structured ASIC. However, recent developments by Xilinx in customer-specific FPGAs now preserve some of the flexibility of the FPGA while also maintaining a low-cost approach.

Xilinx Spartan-3 and Virtex™-4 EasyPath FPGAs enable you to prototype two different designs in a standard FPGA and then move to an EasyPath device that supports both those designs simultaneously in production. For example, you can use one bitstream to perform system diagnostics on the entire system and the other to load the second application-specific bitstream. Alternatively, you can choose to implement designs for two different products in a single device and take advantage of a common part number for inventory management purposes.

In addition, with Spartan-3 and Virtex-4 EasyPath FPGAs, you can change LUTs and I/Os even after these devices have been deployed in the field (see Figure 3). As a result, you can now fix minor bugs or tweak certain parameters to further optimize your designs.

For instance, a line card in a router might need to have the drive strength (and slew rate) adjusted a notch or two depending on what load it encounters. You can implement a range of drive strengths that are available

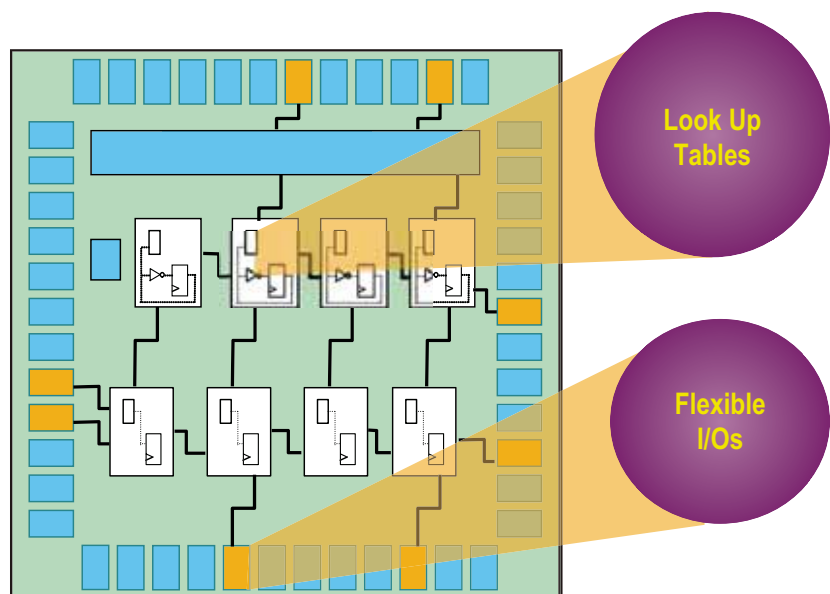


Figure 3 – EasyPath FPGAs allow ASSP customers to fix minor design bugs by changing LUTs and I/Os even after they are in high-volume production.

for certain I/Os. This new level of customer-specific flexibility offers a unique blend of FPGA-like features at ASIC-like prices.

Another important issue is the availability of qualified, reliable IP. ASSP vendors can take advantage of the vast portfolio of IP offered by FPGA vendors during the prototyping phase. When the design is ready for production, you can use the same IP without any additional charges or qualification effort. ASIC solutions, on the other hand, require ASSP vendors to either maintain their own portfolio of state-of-the-art IP or incur large expenditures in acquiring/qualifying standard IP blocks.

### Case Study: Consumer Electronics

Companies developing consumer electronic products increasingly find themselves having to incorporate more and more functionality while maintaining lower costs. In no other area are these trends more evident than in home networking, which involves the aggregation and distribution of content within a home through wireless modems, cable, xDSL, and satellite set-top boxes, among others.

In these applications, the ability of chipset vendors to integrate various standards and encrypt/decrypt data streams is critical. Xilinx Spartan-3 FPGAs (and their EasyPath analogs) support multiple I/O standards such as Ethernet, IEEE-1394, USB2.0, and PCI, allowing you to develop designs that are either feature-rich or segmented by end usage without any additional effort. The Spartan-3 family also offers an extensive library of encryption cores such as AES, DES, and TDES for applications where security is important.

In addition, Spartan-3 EasyPath FPGAs support various SSTL and HSTL I/Os for interfacing to different high-speed memories such as SRAM and DRAM, as well as reduced swing differential signaling (RSDS), with applications in LCD TVs and other display products where power consumption is critical.

Finally, for applications that require computational capability like image/video processing, the Spartan-3 EasyPath FPGA's MicroBlaze™ soft-processor cores bring the MIPS cost down below \$0.02 per DMIP,

while at the same time keeping the core area to about 1% in an XC3S5000. This provides you with low-cost processing power while leaving enough room for other peripherals. For example, at a unit cost of \$12.95 (the 50K unit price) for an EasyPath XC3S1500 device, you can prototype with confidence using Spartan-3 standard FPGAs and convert to EasyPath FPGAs for high volume.

### Conclusion

Power, performance, and cost have ranked high among the reasons why ASSP vendors have historically migrated to ASIC solutions over FPGAs. But recent advances in process technologies have significantly mitigated these concerns to a point where solutions like EasyPath FPGAs have become viable high-volume ASSP alternatives.

The use of triple-oxide technology, for example, has allowed Xilinx to selectively vary gate-oxide thicknesses to optimize specific regions for low power or high per-

formance. As a result – and contrary to industry trends – static power consumption in the Xilinx 90 nm Virtex-4 family is about 50% lower than in 0.13μm FPGA devices.

On the performance front, the use of specialized embedded hard macros for processor cores and DSP slices allows Xilinx to provide operating frequencies on par with ASICs. Even on the cost front, the move to smaller process nodes and the development of clever techniques to improve yields has allowed FPGA vendors to shift the crossover point between FPGAs and ASICs to higher and higher volumes.

ASSP vendors are being squeezed from both ends – by market uncertainties and risk on one side and rising product development costs on the other. EasyPath FPGAs offer a way out. They eliminate the risk of a new product introduction by significantly reducing the total cost of development and the time to production. ASSP vendors can now address many more markets and segments that might otherwise have been uneconomical. ●●●

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