

To Interleave, or Not to Interleave: That is the Question

Controlling crosstalk in PCI Express and other RocketIO implementations.

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With the emergence of multi-gigabit-per-second SERDES bus architectures such as PCI Express, Xilinx® RocketIO™ technology has become a vital part of FPGA designs. But accompanying these faster buses is a resurgence of an old design problem: crosstalk. The source of concern is similar to what occurs in buses like PCI and PCI-X: a large number of signals all need to go to the same place, from the FPGA to a connector or to another chip.

The bad news is that PCI Express edge rates are much faster than PCI and PCI-X. The fastest edges can be on the order of 50 ps, which equates to around a third of an inch on a printed circuit board. This equates to more crosstalk for a given amount of parallelism, which can be quite large for typical PCI Express link lengths.

The good news is that because PCI Express links comprise unidirectional differential pairs, you only need to control crosstalk at the receiver. This characteristic of PCI Express has actually led to two theories on how to implement board routing: interleaving TX and RX pairs or keeping like pairs together. There is no one correct answer to this design question; the answer depends on the characteristics of the design.

FEXT, NEXT, and Interleaving

In order to determine the best method for routing adjacent PCI Express differential pairs, you should understand the nature of both forward and reverse crosstalk. Both types of crosstalk are caused by coupling between traces; that coupling includes mutual inductance as well as mutual capacitance.

In forward crosstalk, also referred to as far-end crosstalk or FEXT, coupled energy propagates onto the “victim” signal in the same direction as the “aggressor” signal. As such, the FEXT pulse has an edge equivalent in length to the aggressor signal and continues growing in amplitude as the signals propagate down the line. The amplitude of FEXT is thus determined by the

length of parallelism between adjacent traces and the amount of coupling, as well as the balance between the inductive and capacitive components of coupling.

In reverse crosstalk, also known as near-end crosstalk or NEXT, the coupled energy propagates in the opposite direction of the aggressor signal. As such, its amplitude is also length-dependent, but saturates for any coupled length greater than the signal edge rate. In NEXT, the inductive and capacitive coupling are additive.

Figure 1 shows examples of these two types of crosstalk in the Mentor Graphics HyperLynx oscilloscope. Notice how the forward crosstalk (shown in light blue) is a large spike whose leading edge has an edge rate equivalent to that of the aggressor signal (in this case 100 ps). The reverse crosstalk (shown in yellow) is much smaller in amplitude, with a width equal to twice the total line length (in this case, 5 inches or 712 ps). The topology used to generate these waveforms in HyperLynx LineSim is depicted in Figure 2.

You can reduce the coupling between traces most effectively by increasing the spacing between them. Because PCI Express comprises unidirectional differential pairs, you can further control crosstalk by altering the aggressors' direction to allow for only reverse crosstalk or only forward crosstalk.

For trace configurations where the forward crosstalk exceeds the reverse crosstalk, the preferred method of routing differential pairs would be to interleave them. If a TX signal is placed adjacent to an RX signal, the forward crosstalk created by that signal will go towards the transmitter of the RX signal, where it is not of concern. The reverse crosstalk created by the TX signal will go towards the receiver of the RX signal.

Conversely, if the reverse crosstalk exceeds the forward crosstalk, non-interleaved routing would be preferable; all forward crosstalk would be directed towards the victims' receivers instead of the reverse crosstalk.

Microstrip and Stripline Crosstalk Analysis

To determine when each method of routing is appropriate, let's examine both inner and outer layer routing in simulation with a topology similar to that shown in Figure 2. In the first example, a set of three microstrip differ-

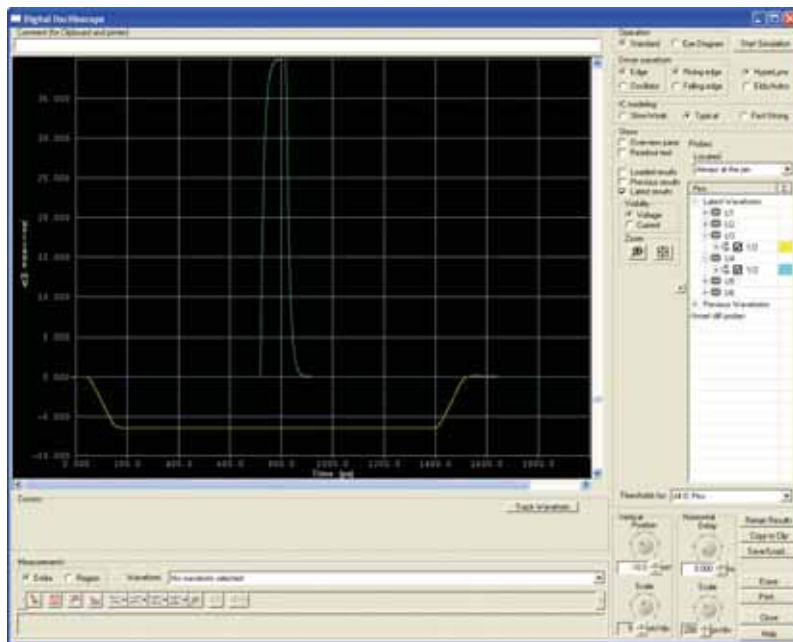


Figure 1 – Forward and reverse crosstalk

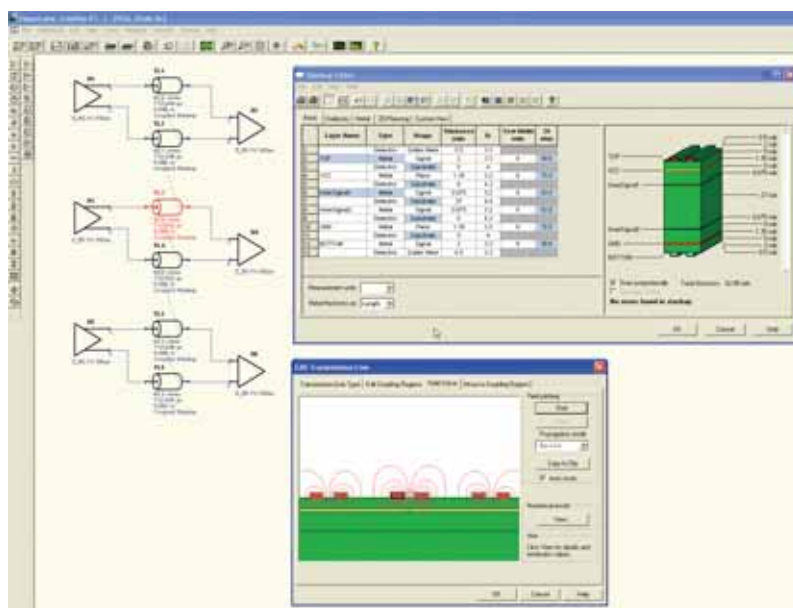


Figure 2 – Topology used for crosstalk analysis

ential pairs, with 5-mil wide copper traces 2 mils thick separated by 5.7 mils, sitting on a 5-mil dielectric with an $\epsilon_r = 4$, covered with a 0.5-mil solder mask with an $\epsilon_r = 3.3$, have their spacing and lengths varied in simulation to obtain the information shown in Table 1.

In microstrip routing, far-end crosstalk dominates, except in the very rare case of super-short routing and super-tight spacing. As such, it would be reasonable to

make a general rule that PCI Express pairs should be routed as interleaved when being routed on microstrip.

In the second example, three stripline (inner-layer) differential pairs, with 4-mil wide copper traces 2 mils thick separated by 5.0 mils, in a dual-stripline configuration with dielectric heights of 4, 20, and 4 mils, all modeled with an $\epsilon_r = 3.5$, have their spacing and lengths varied in simulation to obtain the information shown in Table 2.

Notice that the far-end crosstalk is 0 mV. This is because of the balance that exists between the counteracting capacitive and inductive couplings on the homogenous stripline. This might lead you to believe that non-interleaved routing should always be used on the stripline. However, that would be an erroneous assumption. Homogenous stripline rarely exists on a real printed circuit board. There are differences in dielectric constants between cores and prepregs, the two types of dielectrics that make up a stripline. Furthermore, there are resin-rich areas localized to the traces that alter the dielectric constant around the traces. To properly determine whether or not to interleave stripline traces, you must appropriately model the dielectric constants.

The third example uses the same dual stripline trace configuration, except that the two 4-mil dielectrics are assigned an $\epsilon_r = 3.5$, the 20-mil dielectric an $\epsilon_r = 4.5$, and the thin layer of dielectric on the signal layer is given an $\epsilon_r = 3.2$. Differential pair spacings and lengths are varied to produce the results shown in Table 3.

From this data, it is evident that on longer buses, or buses with longer amounts of parallelism, you should use interleaved routing because far-end crosstalk dominates. Near-end crosstalk dominates for shorter routes with tighter spacings. The point at which the far-end crosstalk exceeds the near-end crosstalk varies based on length, spacing, and trace configuration. That crossover point is what you should use to determine whether or not to interleave TX and RX differential pairs.

Conclusion

Clearly, the majority of board routing implementations for PCI Express and similar RocketIO implementations requires that you interleave TX and RX differential pairs in the layout. This is certainly true for microstrip, where forward crosstalk dominates. It is also true for stripline, with the exception of tighter spacing with shorter lengths. That is because forward crosstalk is non-zero in an actual stripline, and will in many cases exceed reverse crosstalk. Simulation, with proper modeling of the stripline dielectrics, reveals this phenomenon, while pinpointing the trace configuration where the FEXT will exceed the NEXT and indicate whether or not to interleave.

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	1H	2H	3H	5H
1 in.	NEXT = 75 mV, FEXT = 25 mV	NEXT = 27.9 mV, FEXT = 18 mV	NEXT = 12.7 mV, FEXT = 12 mV	NEXT = 3.7 mV, FEXT = 5.4 mV
2 in.	NEXT = 75 mV, FEXT = 47 mV	NEXT = 27.9 mV, FEXT = 37.8 mV	NEXT = 12.7 mV, FEXT = 24 mV	NEXT = 3.7 mV, FEXT = 10.5 mV
5 in.	NEXT = 75 mV, FEXT = 125 mV	NEXT = 27.9 mV, FEXT = 94 mV	NEXT = 12.7 mV, FEXT = 62 mV	NEXT = 3.7 mV, FEXT = 26 mV
10 in.	NEXT = 75 mV, FEXT = 255 mV	NEXT = 27.9 mV, FEXT = 192 mV	NEXT = 12.7 mV, FEXT = 126 mV	NEXT = 3.7 mV, FEXT = 53 mV
20 in.	NEXT = 75 mV, FEXT = 508 mV	NEXT = 27.9 mV, FEXT = 381 mV	NEXT = 12.7 mV, FEXT = 254 mV	NEXT = 3.7 mV, FEXT = 105 mV
30 in.	NEXT = 75 mV, FEXT = 625 mV	NEXT = 27.9 mV, FEXT = 555 mV	NEXT = 12.7 mV, FEXT = 379 mV	NEXT = 3.7 mV, FEXT = 158 mV

Table 1 – Crosstalk in terms of differential pair spacing versus trace length for a microstrip configuration

	1H	2H	3H	5H
1 in.	NEXT = 72.1 mV, FEXT = 0 mV	NEXT = 29.9 mV, FEXT = 0 mV	NEXT = 14.5 mV, FEXT = 0 mV	NEXT = 4.5 mV, FEXT = 0 mV
2 in.	NEXT = 72.1 mV, FEXT = 0 mV	NEXT = 29.9 mV, FEXT = 0 mV	NEXT = 14.5 mV, FEXT = 0 mV	NEXT = 4.5 mV, FEXT = 0 mV
5 in.	NEXT = 72.1 mV, FEXT = 0 mV	NEXT = 29.9 mV, FEXT = 0 mV	NEXT = 14.5 mV, FEXT = 0 mV	NEXT = 4.5 mV, FEXT = 0 mV
10 in.	NEXT = 72.1 mV, FEXT = 0 mV	NEXT = 29.9 mV, FEXT = 0 mV	NEXT = 14.5 mV, FEXT = 0 mV	NEXT = 4.5 mV, FEXT = 0 mV
20 in.	NEXT = 72.1 mV, FEXT = 0 mV	NEXT = 29.9 mV, FEXT = 0 mV	NEXT = 14.5 mV, FEXT = 0 mV	NEXT = 4.5 mV, FEXT = 0 mV
30 in.	NEXT = 72.1 mV, FEXT = 0 mV	NEXT = 29.9 mV, FEXT = 0 mV	NEXT = 14.5 mV, FEXT = 0 mV	NEXT = 4.5 mV, FEXT = 0 mV

Table 2 – Crosstalk in terms of differential pair spacing versus trace length for a homogenous stripline configuration

	1H	2H	3H	5H
1 in.	NEXT = 78.4 mV, FEXT = 5.2 mV	NEXT = 34 mV, FEXT = 5.2 mV	NEXT = 17.2 mV, FEXT = 3.5 mV	NEXT = 5.6 mV, FEXT = 3.6 mV
2 in.	NEXT = 78.4 mV, FEXT = 9.5 mV	NEXT = 34 mV, FEXT = 10.1 mV	NEXT = 17.2 mV, FEXT = 7 mV	NEXT = 5.6 mV, FEXT = 3.6 mV
5 in.	NEXT = 78.4 mV, FEXT = 18.2 mV	NEXT = 34 mV, FEXT = 21.5 mV	NEXT = 17.2 mV, FEXT = 17.4 mV	NEXT = 5.6 mV, FEXT = 10.8 mV
10 in.	NEXT = 78.4 mV, FEXT = 34.8 mV	NEXT = 34 mV, FEXT = 42.8 mV	NEXT = 17.2 mV, FEXT = 34.6 mV	NEXT = 5.6 mV, FEXT = 19.7 mV
20 in.	NEXT = 78.4 mV, FEXT = 67.1 mV	NEXT = 34 mV, FEXT = 82.1 mV	NEXT = 17.2 mV, FEXT = 70.5 mV	NEXT = 5.6 mV, FEXT = 39.2 mV
30 in.	NEXT = 78.4 mV, FEXT = 101.4 mV	NEXT = 34 mV, FEXT = 124.8 mV	NEXT = 17.2 mV, FEXT = 104 mV	NEXT = 5.6 mV, FEXT = 58.6 mV

Table 3 – Crosstalk in terms of differential pair spacing versus trace length for a realistic stripline configuration