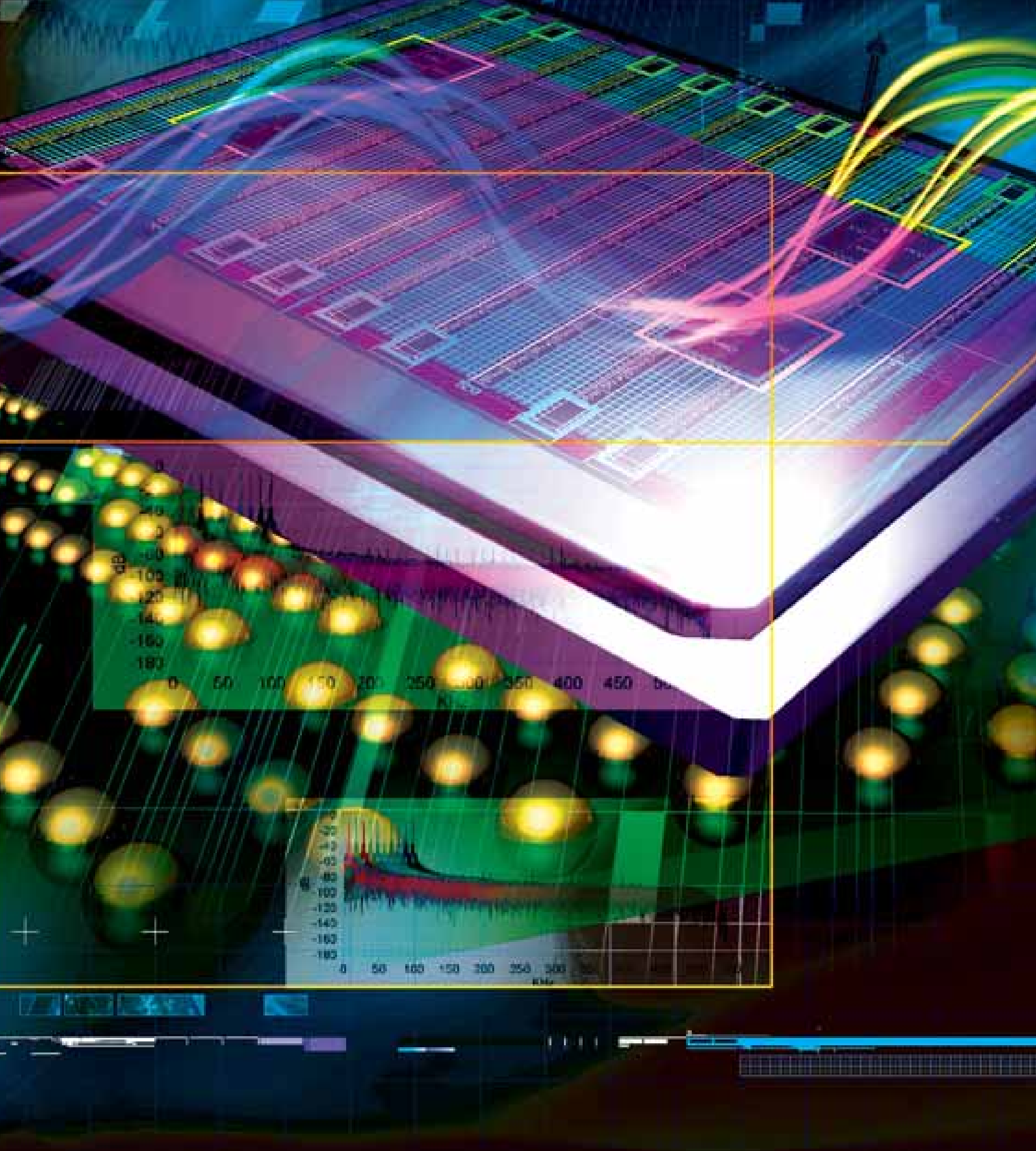
II DRR Delivers High-Performance SDR

Innovative Integration utilizes Virtex-II Pro FPGAs for a software-defined radio receiver system.



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Innovative Integration (II) Inc. has developed a powerful solution for multi-channel software-defined radio (SDR). The II digital radio receiver (DRR) has a wide-bandwidth IF front-end digitizer integrated with Xilinx® Virtex™-II Pro FPGAs. This configuration allows you to realize the full flexibility of scalable programmable design with high-performance signal processing hardware.

Using MATLAB's Filter Design and Analysis tool (FDATool) and Innovative's FrameWork Logic software, you can easily design and optimize your desired filters.

You can customize and optimize the II DRR for multiple applications using the II SDR reference design. The reference design incorporates a MATLAB Simulink environment with Xilinx System Generator for DSP. In the System Generator tool, data is bit- and cycle-true and reflects the performance of the real system. You can easily modify the characteristics of the system by changing the parameters in the blocksets. You can then verify the blocksets in real-time simulations. Four Texas Instruments (TI) 1 GHz TMS320C6416 DSPs supply ample calculating power for advanced operations such as signal encoding, decoding, and compression.

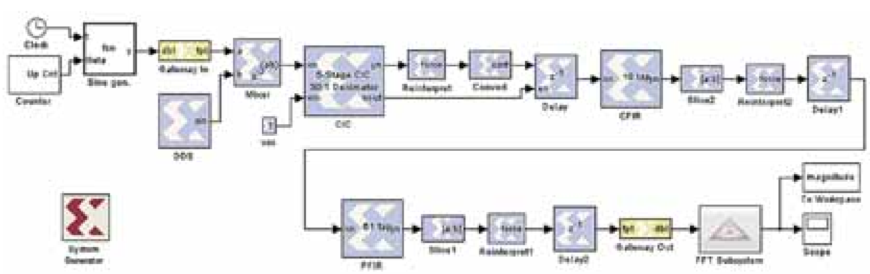

Figure 1 – Simulink block diagram of DDC using Xilinx System Generator software

Anatomy of a Digital Down Converter

In the II DRR system, a digital down converter (DDC) decimates the RF to IF signal, providing signal compensation and shaping. The DDC comprises a cascaded integrator-comb (CIC) filter, a compensation filter (CFIR), and a programmable filter (PFIR).

The CIC filter is useful to realize large sample rate changes in digital systems. A CIC filter is a "multiplier-less" structure that comprises only adders, subtractors, and registers, which facilitates hardware implementation. The compensation filter flattens the passband frequency response. The programmable low-pass filter lowers the magnitude of the ripples produced by the CIC filter.

Figure 1 shows the entire SDR signal processing for the DDC. The channel filtering is built in the MATLAB Simulink environment using the SDR blockset. The input signal is tuned to the target frequency using a mixer and a direct digital synthesizer (DDS). The signal then flows through the CIC, CFIR, and PFIR.

You can implement the SDR directly in hardware by using the Xilinx System Generator tool to generate the signal processing logic that is fit into the Virtex-II Pro FPGA using Xilinx ISE™ software. The whole system can be designed and downloaded to hardware in hours, which effectively shortens time to market.

Designing Channel Filters

Using MATLAB's Filter Design and Analysis tool (FDATool) and Innovative's FrameWork Logic software, you can easily design and optimize your desired filters.

Consider a GSM system where the filter specification is:

Fs/2=32.5 MHz, Fpass=0.49 MHz,
Fstop1=0.542 MHz, Fstop2=1.35 MHz

The sampling frequency is 130 MHz and the decimation factor is 120. Figure 2 shows the theoretical system response from 0 Hz to 65 MHz.

When the specified filter is simulated, the passband ripple is within -0.8 dB, as shown in Figure 3a. Likewise, the magnitude is down to -40 dB at 0.544 MHz and below -90 dB after 1.365 MHz, as shown in Figure 3b.

The channel filter design verified in the simulation is bit- and cycle-true – so the DDC design matches the theoretical expected response shown in Figure 2.

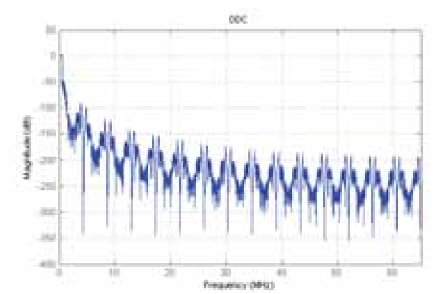

Figure 2 – Theoretical frequency response of DDC of R = 120 from FDATool program

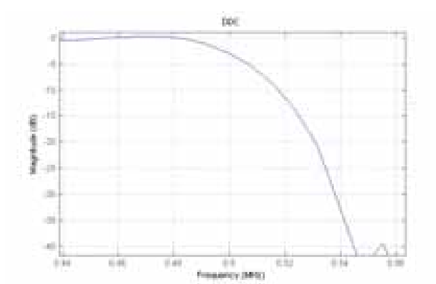

Figure 3(a) – Frequency response at the corner of Fpass = 0.490 MHz

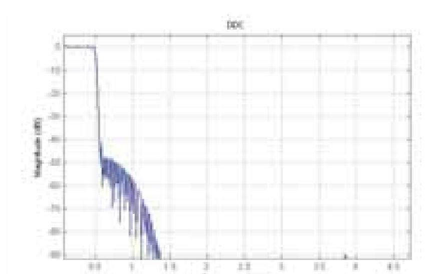

Figure 3(b) – Frequency response within 0.5 MHz

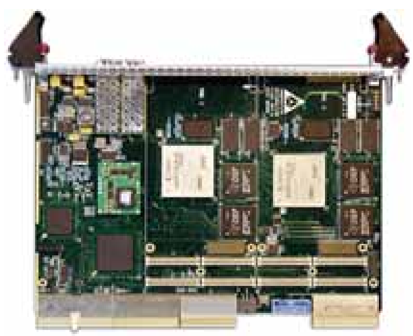

Figure 4 – Quadia DSP/FPGA card with dual Xilinx FPGAs and four TI DSPs

Figure 5 – UWB PMC module with dual 250 MSPS A/Ds

II DRR Implemented in Hardware

The II DRR system comprises one Quadia DSP card and two ultra-wideband (UWB) PMC I/O modules that can perform digital down conversions and channel filtering on 40 channels simultaneously. The high-speed, front-end signal processing for the DRR is implemented in Virtex-II Pro XC2VP40 FPGAs on the Quadia card and UWB modules, as shown in Figures 4 and 5.

The Quadia card has four TI 1 GHz TMS320C6416 DSPs that are used for baseband processing. The DRR has 40 independently tuned channels that deliver captured in-phase and quadrature (IQ) data to the DSPs. The FPGAs implement 16 MB data queues for each channel with flow control to the DSPs. This configuration allows the DRR to efficiently process the large data rates of the DRR system.

The II DRR system was tested to show channel filter response, system frequency response, and signal quality – and demonstrated excellent results. The results closely matched the theoretical performance predicted by the MATLAB simulations. Each output channel has a tuning resolution of 10 kHz and a noise floor of around -90 dB. The system dynamic range was shown to be greater than 80 dB.

Customize Your Applications

More than 40 percent of the Virtex-II Pro logic blocks and four high-throughput DSP chips are available for your custom applications. The software provided for the II DRR system supports the complete configuration of your system. The software also supports using the DSPs on the Quadia board for channel baseband processing.

The DRR system supports either a single pair of DSPs or a full configuration with four DSPs and two UWB modules. It also supports logic and DSP program downloads to all of the devices in the system through a host PCI. This allows dynamic reconfiguration of the system for multi-protocol applications.

C++ development libraries on both the host and target DSPs are provided to perform hardware and data-flow management. Most system operations – including data transfer from target to host, loading system logic, and DSP common object file format (COFF) file downloading – can be performed with a single function call using Innovative's Malibu host library. DSP functions, including device drivers for the DRR interface and controls, are included in Innovative's Pismo library and run under TI's DSP/BIOS RTOS.

An advantage of the Malibu library is that the code to control the baseboards is standard C++ code, and the library is portable between different compilers. The Malibu library supports Borland C++ Builder 6 and Microsoft Visual Studio 2003.

The configuration software allows the setup of each channel on the DRR. You can configure each channel to have its own A/D input, tuning frequency, gain, and spectral inversion. Tuning frequencies are saved relative to a base frequency. This base frequency can be measured in calibration and loaded into the program to allow selection of precise tuning frequencies. All configurations and settings may be saved and reloaded for convenience.

Once the configuration is set, you can download selected target programs to the designated DSPs. A global trigger to the system for all channels begins data flow in the system. The DSPs continuously process data from the DRR and deliver the data to the host.

Conclusion

Innovative Integration's digital radio receiver system is a practical multi-channel SDR application that takes you step-by-step from requirements to implementation. Using MATLAB Simulink DSP tools to define specific digital signal processing, you can directly – and quickly – implement your SDR model into Xilinx Virtex-II Pro FPGAs and TI DSPs using Xilinx System Generator and ISE software. The final hardware is realized on Quadia DSP cards and UWB PMC modules using Innovative's comprehensive FrameWork Logic system and DSP software support.

Everything you need to produce a working SDR application based on the II DRR system model is available through the Innovative Integration website at *www.innovative-dsp.com.*