Samsung QDR II SRAM

The Samsung QDR II SRAM is a good fit for Virtex-5 devices.

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To meet increasing demand for high-bandwidth performance in private and public networking, Samsung Semiconductor recently introduced QDR II specialized memory products designed to optimize system-configuration bandwidth (Table 1). At 300 MHz, Samsung's QDR II SRAM offers one of the highest transmission speeds available today, and also provides an optimal transmission solution when used in conjunction with the Xilinx® Virtex™-5 system integration platform.

Samsung offers a broad portfolio of QDR II solutions, primarily at speeds of 250 MHz and 300 MHz and densities of 72 Mb or less. Samsung QDR II products are based on a common industry specification developed by the QDR SRAM Consortium. Because the consortium pursues an aggressive evolution for memory speeds in network applications, leading-edge QDR II/DDR2 product lines such as Samsung's are widely found today in routers, switches, and related networking equipment.

QDR II Memory

The efficiency of Samsung's 300 MHz QDR II memory takes full advantage of the features and functionality of the Virtex-5 FPGA platform. The Virtex-5 FPGA enables wider and faster interface transfers for QDR II memory architectures with a data rate of 600 Mbps, bandwidth at 389 Gbps, and a data width of 2 x 324 (number of bits).

The QDR II provides an aggregate throughput of 56.7 Gbps per pin for a 36-bit write bus and a 36-bit read bus operating in DDR mode, with a data valid window set at 65% of the input clock cycle.

Samsung's QDR II SRAM can perform two data writes and two data reads in a burst-of-four per clock cycle at the 300-MHz bandwidth. Its unidirectional data ports support simultaneous reads and writes and allow back-to-back transactions without any bus contention issues. For power, the QDR II SRAM device uses either the 1.5V or 1.8V HSTL I/O standard.

The QDR II memory supports simultaneous high-speed read and write operations through separate input and output ports at the same cycle as the Virtex-5 device. Memory bandwidth is maximized because data is transferable from the controller to the SRAM at every rising edge of the K and /K clock cycles and moved out of the SRAM on every rising edge of the C and /C cycles. The Virtex-5 device's highly integrated independent functionality provides continuous read and write ports for the transfer of data, eliminating the need for a bus turnaround every cycle.

Power Supply	1.8V +/- 0.1V
Circuitry	DLL for wide output data-valid window and future frequency scaling
Data Ports	Separate independent read and write data ports with concurrent read and write operation HSTL I/O
I/O	1.5V/1.8V HSTL I/O
Read/Write	Synchronous pipeline read with self-timed early write
Interface	Double data rate (DDR) on read and write ports
Clocks	Two input clocks (K and /K) for DDR timing at rising edges Two input clocks (C and /C) for output data to minimize skew Two echo clocks (CQ and /CQ) to enhance output data trace
Package	165 FBGA (11 x 15 ball array) with body size of 15 x 17 mm and lead-free

Table 1 – Samsung QDR II SRAM features

Burst-of-Four QDR II SRAM Devices

Samsung's burst-of-four QDR II SRAM device supports four-word data transfers on all write and read activity. This effectively reduces addressing activity, allowing substantially more data to be transmitted every second. The Virtex-5 FPGA is designed to control a burst-of-four-words at every clock cycle.

Samsung QDR II SRAM Functionality

Figure 1 shows how a burst of four is transmitted by the QDR II SRAM for all write and read activity. The size of each address, data-in bus, and data-out bus is kept at an entire clock cycle and depends on the performance capability of the Samsung QDR II, as well as how efficiently it connects with Virtex-5 interfaces. As many as 20 additional data blocks can be transferred per clock cycle at the QDR II's highest speed of 300 MHz, compared to the previous highest speed of 250 MHz.

Multiple QDR II SRAM

You can increase the cost-effectiveness of your data transmission circuit by using multiple QDR II SRAM memory devices concurrently. There are three reasons for this:

1. To increase the memory's density beyond 72 Mb
2. To easily expand the depth of the memory resource
3. To attain higher bandwidth – as high as 56.2 Gbps

Figure 2 shows how you can connect an unlimited number of SRAM memory devices together to maximize the amount of bandwidth in a transmission.

The Virtex-5 platform generates all clock and control signals for the QDR II's data-read and data-write functions. Each memory clock function is generated using a DDR register. The Virtex-5 device's address and control signals easily meet all requirements for transmitting each data block.

Power-Up/Power-Down Supply Voltage Sequencing

If a system has an unstable clock stage after initial power-up, Samsung recommends the following sequence of power-up supply voltages: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and V_{IN}. You can apply the V_{DD} and V_{DDQ} voltages simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up.

If the clock becomes unstable, Samsung recommends the following power-down supply voltage removal sequence: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, and V_{SS}. You can remove V_{DD} and V_{DDQ} simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

Conclusion

In this article, I've described specification and timing details of a burst-of-four Samsung QDR II SRAM interface connected through a Virtex-5 device. The Virtex-5 device provides the highest possible performance and one of the most scaleable memory interface solutions today for current and next-generation QDR II SRAM memory.

The advantage of QDR II SRAM is that it gives a total throughput of 56.7 Gbps per pin for a 36-bit write and 36-bit read bus at 300 MHz, with a data valid window at 65% of the input clock cycle. At this time, Samsung has found no better configuration for optimizing network traffic flow.

For more information, visit *www.qdrsram.com.*

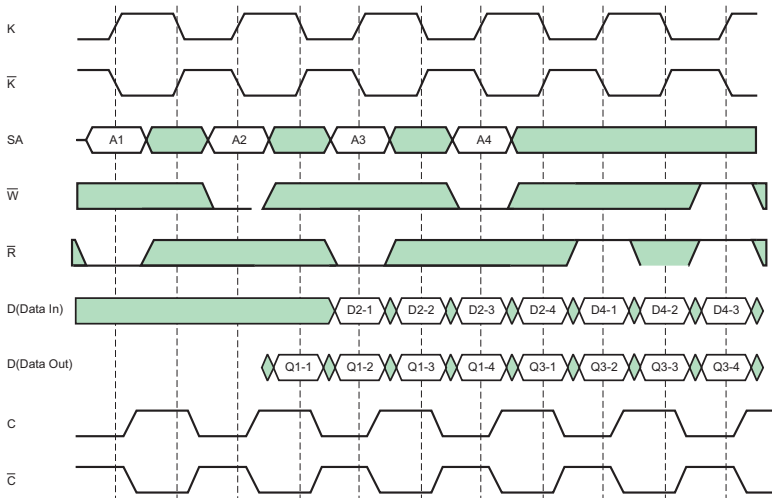

Figure 1 – Burst-of-four QDR II SRAM timing diagram

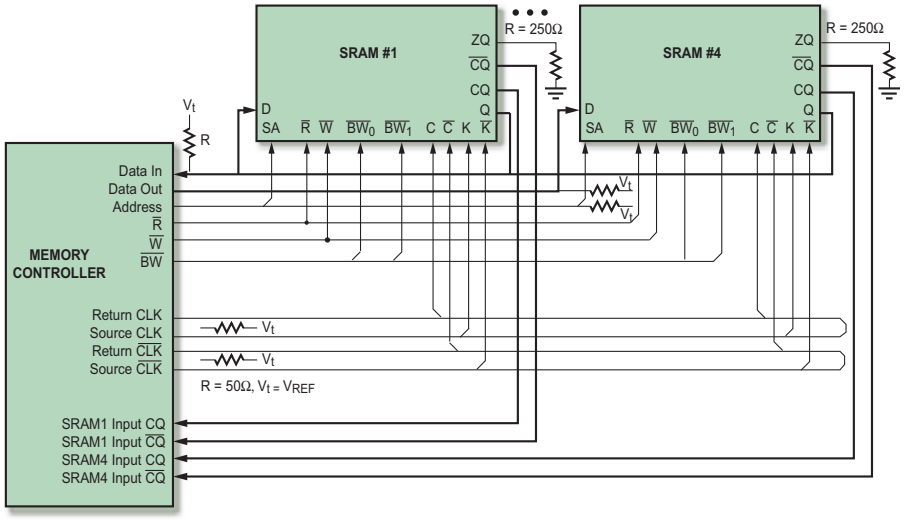

Figure 2 – Schematic of multiple QDR SRAM