



Introducing the Virtex-5 FPGA Family

The first 65-nm advanced FPGAs raise the bar in performance, power efficiency, capacity, and value.



by Steve Douglass
Vice President
Product Development,
Advanced Product Division
Xilinx, Inc.
stephen.douglass@xilinx.com

Welcome to the Virtex™-5 issue of *Xcell Journal*. The Xilinx® Virtex-5 family is not only the industry's first 65-nm FPGA – it also offers some of the most advanced architecture and highest performance in the world. Continuing our history of developing groundbreaking technology, we listened to leading design engineers in various markets and built on key characteristics that made our Virtex-4 FPGA family a tremendous success:

- Higher performance
- Higher logic density
- Lower power consumption
- More advanced features

The fundamental value propositions of FPGAs include faster time to market, versatility, support for evolving standards, risk mitigation, field upgradability, and lower system costs. Our FPGAs accommodate your demands for continued improvements in performance, capacity, power consumption, and cost.

The Virtex-5 family combines the inherent advantage of state-of-the-art 65-nm process technology with an innovative design that is based on a deeper understanding of the applications our products serve. In this article, I'll provide an overview of the new features in Virtex-5 devices, explain the underlying technology, and offer a glimpse of the design decisions that led to our world-leading FPGA architecture.

Process Technology and Architectural Innovations

Virtex-5 FPGAs are built on 65-nm triple-oxide technology using our Advanced Silicon Modular Block (ASMBL™) architecture and providing additional levels of system integration. This new family offers an advanced platform that meets the growing need for programmable systems with higher performance, higher density, lower power consumption, and lower overall system cost.

It might be easy to deliver on one or two of these items, but our challenge was to deliver all of them at the same time.

We successfully met those challenges through a combination of advanced IC process development and innovative architecture and circuit design. Introduced in the Virtex-4 family, our proven ASMBL chip layout architecture allows us to provide the optimal mix of required device resources (logic, memory, arithmetic, I/O, and IP), thus creating the ideal combination for four new platforms:

- The LX platform, optimized for high-performance logic
- The LXT platform, optimized for high-performance logic with low-power serial I/O
- The SXT platform, optimized for high-performance arithmetic- and memory-intensive DSP with low-power serial I/O
- The FXT platform, optimized for embedded processing and very high-speed serial I/O

Compared to our Virtex-4 family, Virtex-5 devices offer 30 percent higher average speed and 65 percent higher capacity in the largest device. Dynamic power consumption is reduced by 35 percent and

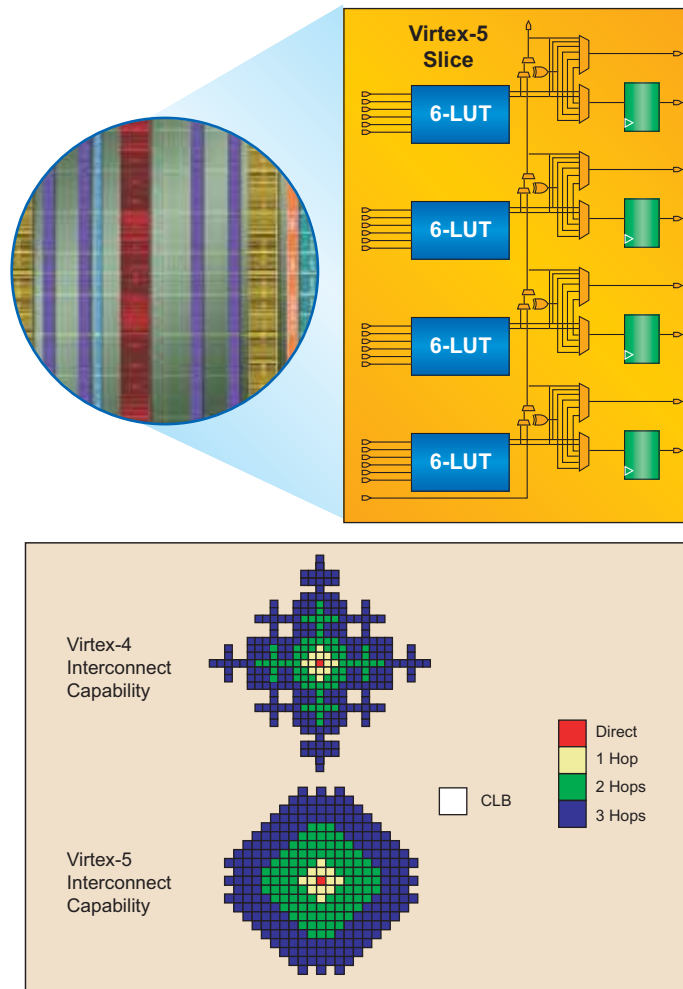


Figure 1 – Virtex-5 ExpressFabric technology

chip area is 45 percent smaller, resulting in a lower cost per function.

Higher Performance and Density

ExpressFabric™ technology implements logic and local interconnect routing. It incorporates look-up tables (LUTs) with six independent inputs, plus a new diagonal interconnect structure, as illustrated in Figure 1. ExpressFabric technology implements combinatorial logic in fewer LUT levels and uses fewer concatenated connections to neighboring building blocks, as compared to the Virtex-4 architecture. This reduces datapath delays and thus increases design performance.

Advanced 6-LUT Logic Structure

For many years, four-input LUTs were the industry standard. However, at 65 nm, the regular structure of the LUT can be shrunk even more than the remaining circuitry

(notably, the interconnect). A six-input LUT (6-LUT) with four times more bits thus increases the CLB area by only 15% – but packs, on average, 40% more logic into each LUT. This higher logic density often reduces the number of cascaded LUTs and can improve the critical path delay, as shown in Figure 2.

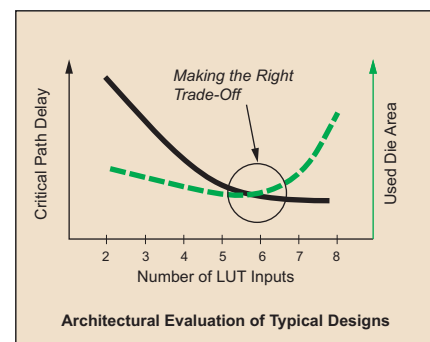


Figure 2 – Optimal performance/area trade-off

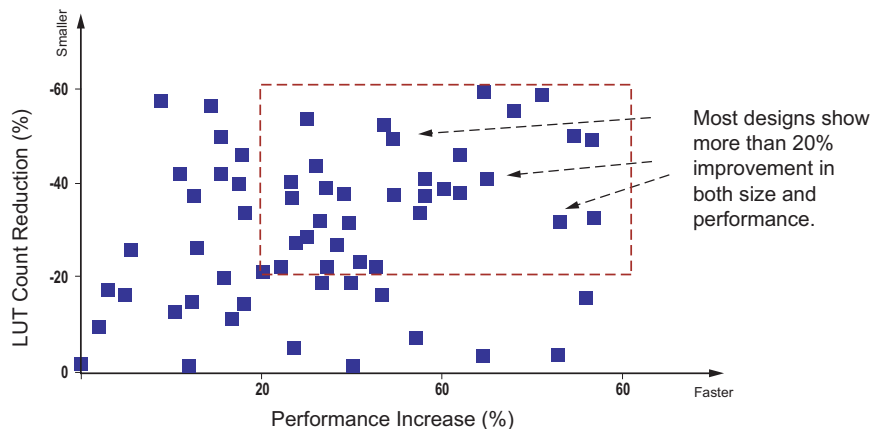


Figure 3 – Virtex-5 FPGA versus Virtex-4 FPGA design suite benchmarks

We took a suite of customer designs and implemented them using ISE™ 8.1i software. For each design, we compared the number of LUTs used with Virtex-4 and Virtex-5 device implementations and correlated this information with the performance increase in megahertz. The scatterplot graph in Figure 3 shows the percentage of performance improvement on the X axis and percentage area savings in terms of LUT count reduction on the Y axis. The new 6-LUT ExpressFabric technology provides a win-win solution in both performance gain and resource savings.

Unlike competing FPGAs, Virtex-5 FPGAs provide real 6-LUTs that you can use as logic or as distributed memories, where a LUT can be a 64-bit distributed RAM (even dual- or quad-ported) or a 32-bit programmable shift register. Each LUT can have two outputs, thus implementing two logic functions of five variables, storing 32 x 2 RAM bits, or acting as a 16 x 2-bit shift register.

New Diagonally Symmetric Interconnect

A new diagonally symmetric interconnect pattern enhances performance by reaching more places in fewer routing hops. A comparison between Virtex-5 and Virtex-4 FPGA interconnect patterns (with each box representing a CLB) is illustrated in Figure 1. The color codes show that with the Virtex-5 FPGA, the pattern is more symmetric, with more CLBs reached in fewer hops. The symmetry thus achieves better results from place and route software tools.

These features are transparent to Virtex-5 FPGA users and are automatically exercised by ISE software, resulting in easier routability and higher overall performance.

Lowest Power Advanced FPGA Solution

The Virtex-5 device family uses our advanced 65-nm, triple-oxide, 11-layer copper CMOS process technology. “Triple oxide” refers to the number of different transistor gate-oxide thicknesses used. The I/O transistors must be 3.3V tolerant and use relatively thick oxide, but the very fast transistors used for logic and other core functions use very thin oxide.

Unfortunately, very thin oxide and very low threshold voltage unavoidably cause high leakage current. There are, however, many transistors in an FPGA that need not be very fast (notably the configuration storage cells). Starting with the Virtex-4 family, Xilinx pioneered a third, intermediate gate thickness for those transistors. This triple-oxide approach allows us to fine-tune the performance and power in the device circuitry; it enables Virtex-5 devices to deliver industry-leading performance while dramatically lowering leakage current and thus static power consumption.

Additionally, the new 6-LUT logic structure combines more logic per LUT, uses fewer local interconnect nodes, and fewer high capacitance nodes between logic functions, reducing the levels of logic and thus the path delay. The new symmetric routing also uses more direct

connects between adjacent logic, again lowering routing capacitance.

V_{CCINT}, the core supply voltage, is now 1.0V. All of these factors contribute to a reduction in overall dynamic power consumption. With the success of the Virtex-4 family, we know that many engineers view performance and power consumption as two equally important constraints in their system designs; therefore, we need to offer both high performance and low power.

We completely reengineered the Virtex-5 logic fabric to fully take advantage of the 65-nm triple-oxide CMOS process, resulting in the highest performance fabric ever, with system clock rates in excess of 550 MHz. At the same time, static power is comparable to that of the 90-nm Virtex-4 devices, while dynamic power has been reduced by at least 35%. Just like its predecessor, the Virtex-5 family again provides the lowest power solution of any advanced FPGA family.

Advanced Features for System Integration

In the Virtex-5 family, we have added a phase-locked loop (PLL) to each clock management tile (CMT), which now contains two digital clock managers (DCMs) and one PLL. The CMT thus offers the best of both worlds: the robust versatility and precise incremental phase shift capability of a digital clock manager combined with the jitter reduction from the analog PLL. The largest device in the family has six CMTs capable of generating and manipulating 550-MHz clocks, supporting the performance of Virtex-5 logic and block functions.

Synchronous dual-ported block RAM is an important function. The size of each block RAM has been increased to 36 Kb, but you can also use it as two independent 18-Kb block RAMs. The data bus width is programmable from 1 bit to 36 bits. In simple dual port mode (one port write, one port read) the data bus width can be as high as 72 bits, effectively doubling the data bandwidth. You can turn off unused 18-Kb blocks to save power.

The block RAM has integrated FIFO control logic, simplifying the design of

asynchronous (or synchronous) FIFOs running as fast as 550 MHz without consuming any logic resources.

The 72-bit-wide block RAM now includes 64-bit error checking and correction (ECC) control logic. Like the integrated FIFO support, the integrated ECC improves memory performance and eliminates the cost associated with traditional fabric-based solutions. You can also use the dedicated ECC logic to augment external memory interfaces.

Interfacing to external devices and especially external memory such as DDR, DDR2, QDR II, and RLDRAM II is dramatically enhanced and simplified by our new ChipSync™ technology. A memory development system (ML561) based on our LX50T devices contains fully functional and hardware-proven reference designs for all of today's most popular memory technologies.

In the DSP domain, we are now providing 25 x 18-bit multipliers, mainly for more efficient floating-point designs. These DSP48E slices can be directly cascaded for higher performance in digital filtering or video broadcast applications. Direct cascading also saves power – as much as 40% compared to competing solutions.

Virtex-5 SelectIO™ technology continues to lead the industry. Every pin supports virtually every I/O standard in use today and offers up to 1.25 Gbps LVDS and 800 Mbps single-ended I/O performance.

Beyond the IDELAY option, which offers programmable input delay in steps of 75 ps, the new ODELAY option now offers the same fine granularity at the FPGA output. Either of these functions is individually programmable on every device pin.

The IODELAY function is an important feature to enhance reliable transmit and receive of high-speed source-synchronous data and clocks. The intended application includes compensation for board-level skews, bit alignment in a bus, and alignment between data and clock signals. This enables LVDS I/Os to achieve speeds as fast as 1.25 Gbps per pin pair.

Virtex-5 LXT, SXT, and FXT devices also offer embedded serial transceivers –

as many as 24 in the largest LXT device. In designing our fourth-generation RocketIO™ technology of high-speed serial transceivers, we invested significant engineering effort to lower power consumption. At the top speed of 3.2 Gbps, the LXT RocketIO transceiver consumes typically less than 100 mW, making it the lowest power transceiver in any FPGA product (see Figure 4).

Each Virtex-5 LXT RocketIO transceiver is programmable and can implement a myriad of speed and serial standards. Link-layer IP is available for

8,500 LUTs compared to implementation with soft IP.

Virtex-5 devices offer more and smaller I/O banks. The outer I/O banks (as many as eight banks in the largest device) also are arranged to provide a PCB routing advantage that in some cases might save board layers.

To ensure the best simultaneously switching output (SSO) performance and provide the best signal integrity (SI) solution in the FPGA industry, all Virtex-5 devices use Xilinx sparse chevron technology pinout assignments. This ensures that

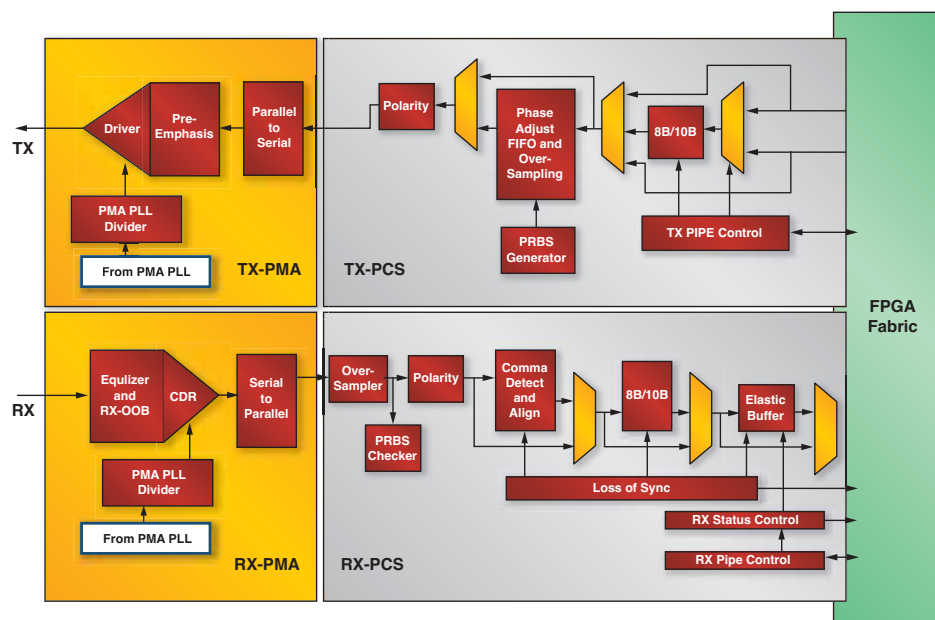


Figure 4 – RocketIO GTP transceiver

such standards as Ethernet, HD/SDI, Serial RapidIO, FibreChannel, and Aurora. Finally, we anticipated the popularity of PCI Express (PCIe) endpoint applications and integrated the complete PCIe endpoint protocol in hard logic. The Virtex-5 LXT PCIe Endpoint block is fully compliant to PCIe standard specification version 1.1 and can support x1, x2, x4, and x8 lane implementations. The integrated hard IP saves logic resources and improves performance for increasingly popular PCIe applications. For an x4 PCIe lane implementation, the Virtex-5 PCIe subsystem block saves as many as

each I/O pin is closely surrounded by power and ground pins, thus minimizing current loop inductance and improving SI.

Conclusion

I hope that you have enjoyed reading about Virtex-5 devices and the factors that drove their design. At Xilinx, we have truly enjoyed the excitement in the system engineering community about this new architecture. We look forward to seeing your next-generation systems benefit from the Virtex-5 enhanced performance and functionality, taking your complex designs to the next level. ●●●