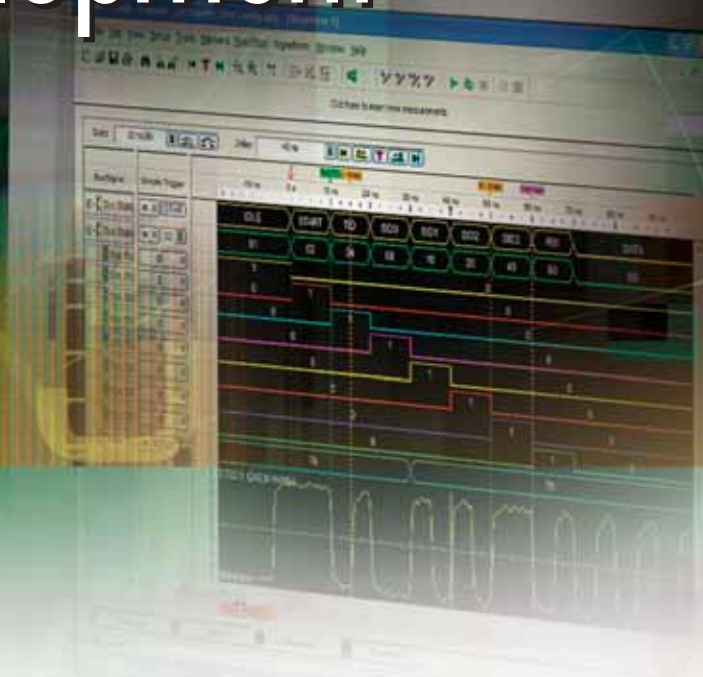


Measurement Cores Shorten Virtex-5 Development

The increase in Virtex-5 performance and flexibility translates into more capable measurement cores to debug complex designs.



by Brad Frieden
Applications Development Engineer
Agilent Technologies
brad_frieden@agilent.com

The introduction of the Xilinx® Virtex™-5 LX family of devices has significantly advanced operation speeds and increased the available resources for FPGAs. As FPGAs have grown in complexity, it is increasingly problematic to manually route-out signals of interest for debugging and validation.

The Virtex-5 family, with up to 330,000 logic cells and 1,200 I/O pins, lends itself extremely well to modern measurement cores and related logic analyzer and mixed signal-oscilloscope FPGA measurement applications. In this article, I'll provide several examples that will help you save significant time in general logic debugging and validation with the MicroBlaze™ version 5.0 soft-processor core.

Measurement Cores and How They Help

The flexibility inherent in FPGAs makes it possible to observe key signals deep inside the circuit. This task can be greatly simplified by tools that automate certain processes, such as mapping the physical connection of FPGA pins to logic analyzer input channels, routing the right FPGA signals out to view, setting up logic analyzer bus and signal names corresponding to those signals, and providing an easy and automated way to route-out new signals of interest. The need for such automated tools grows with the introduction of each generation of successively larger and more complex FPGAs.

One very successful tool that automates signal measurement deep inside the FPGA is a measurement core. A measurement core works in conjunction with a logic analyzer and an FPGA-focused measurement application called the FPGA Dynamic Probe. First, the

measurement core provides the signal MUX functionality to access a lot of signals. Second, the core and analyzer provide a means to detect and keep track of which FPGA pins have probed signals coming out. Third, they allow you to select different signal MUX settings and automatically set up the logic analyzer bus and signal name definitions as they switch between various signal banks.

Figure 1 shows a typical measurement system with a measurement core. A MUX is switched through JTAG and the logic analyzer probes the signals. A capability called "Auto Pin Mapping" wiggles each pin of the FPGA that you have previously defined as a measurement core output, and the logic analyzer scans its input channels until it has found each pin. This greatly simplifies and automates the otherwise tedious and error-prone process of mapping the MUX pins through the device pins and physical probe to the logic analyzer channels.

FPGA pins are usually a precious commodity, so the capability of a Virtex-5 measurement core to map two signals per pin further enhances its value. Time-division multiplexing (TDM) makes this possible. TDM measurement cores are larger and use more resources than simple timing or state cores, but that trade-off can be well worth it. To probe high-speed circuits, you may need to consider certain factors. Figure 2 shows the TDM core architecture and capabilities.

Measurement Core Comparisons

Let's review the size and performance of basic timing, basic state, and pin compression state measurement cores, along with specific logic analyzer probing options including flying leads, Mictor connectors, and SoftTouch connector-less probing. Single-ended versus differential signaling is also a factor in the level of performance that you can achieve.

Core Insertion

The Xilinx ChipScope™ Pro core inserter offers the best means of inserting the measurement core into a design. Figure 3 shows the choices you will have when setting up the interface. These include:

- Capture Mode: timing versus state capture of user signals
- Max Frequency Range: adjustment of pipeline stages to meet timing and lower the load
- ATD Pin Count: the number of FPGA pins dedicated for data, from 4 to 128
- Endpoint Type: single-ended versus differential, depending on signal integrity
- Signal Bank Count: 1, 2, 4, 8, 16, 32, or 64 signal banks
- TDM Rate: 1x, no pin compression; 2x yields two signals per pin
- Data Width: total number of data signals
- Input: FPGA pin locations, I/O standard, drive strength, and slew rate

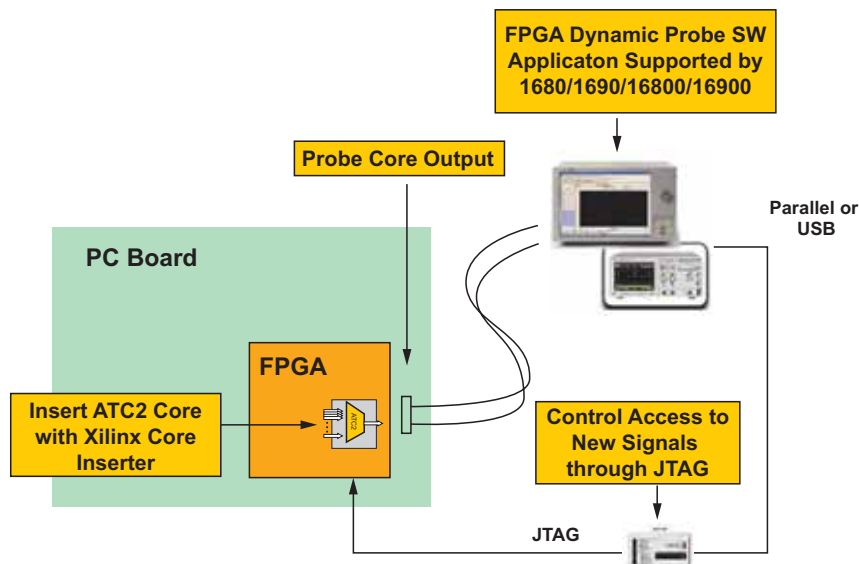


Figure 1 – ATC2 measurement core and FPGA Dynamic Probe

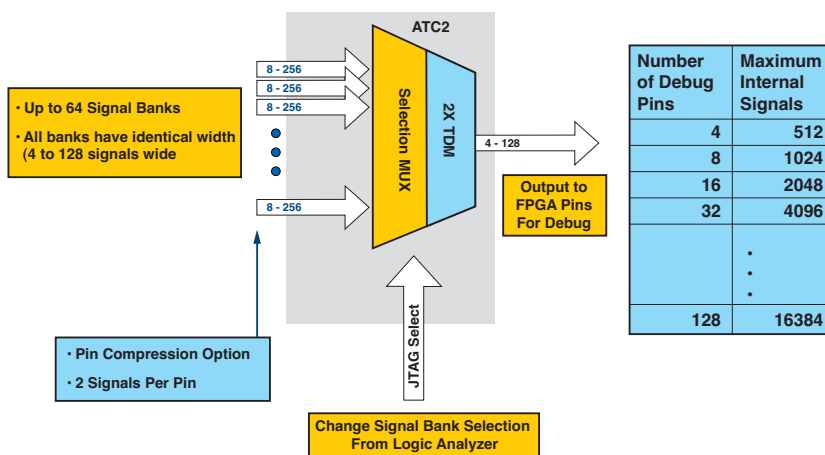


Figure 2 – Time-division multiplexing in ATC2 measurement core

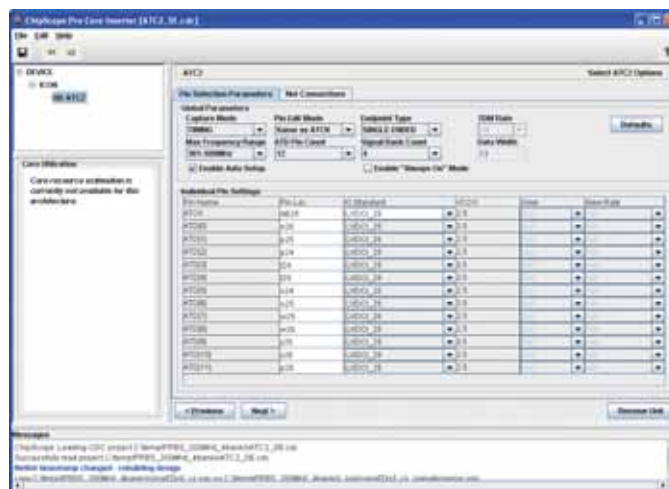


Figure 3 – Core definition choices in ChipScope Pro Core Inserter

Next, you must choose which nets from the design to assign to each signal bank, as shown in Figure 4. Simply refer to the internal nets you wish to probe (as shown in the listing on the left of the display in Figure 4), highlight those nets, and click on the button “Make Connections.”

Core Results

To illustrate the impact of measurement cores on a design, a designer at Agilent inserted each of the four core types, one per test. For each ATC2 core, 4 banks of 12 signals each were defined. For the ILA core, 48 signals were defined. In each case the number of look-up tables and flops required was reported before and after core insertion into a Virtex-5 XC5VLX50 FPGA fabric. The design clock rate was set at 300 MHz (3.33 ns timing constraint). The tools timing report was noted before dropping in a core (1.557 ns) and then again after inserting each core. The results of these tests are summarized in Table 1.

In all cases, with the addition of the measurement core, the designer achieved timing closure and excellent measurements.

2x TDM Core Measurement

To look closely into the 300-MHz clock rate measurement with the 2x TDM state core example, I recommend running a calibration process called EyeFinder. This process determines where the optimal logic analyzer sample point is located for each data bit relative to the defined clock. For the 2x TDM state core, this is the rising edge of the clock for one net and the falling edge of the clock for a second net, with both net signals routed out through one pin. An automatic process then adjusts the logic analyzer sample points and voltage thresholds to optimal positions.

Additionally, a feature called EyeScan can give a rough view of the signal integrity and timing of the signals being probed, as shown in Figure 5. The resulting 300-MHz state capture is shown in Figure 6 using the Agilent 16901A system logic analyzer with a 16950B acquisition module.

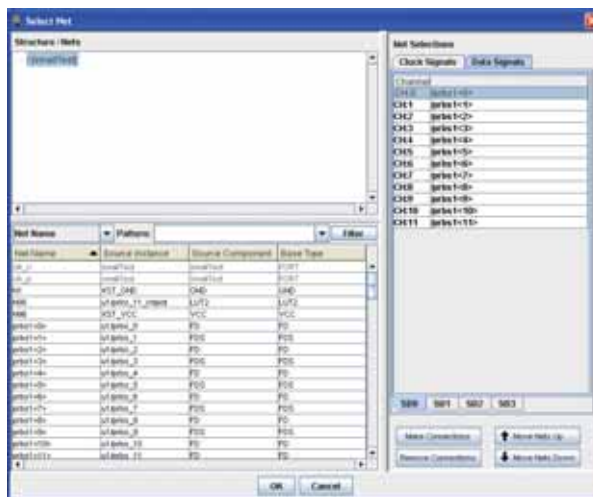


Figure 4 – Signal bank net assignments

	ILA Core, 48 Wide Data, 1k Deep	ATC2 Timing, 13 Wide, 4 Banks	ATC2 State, 12 Wide, 4 Banks	ATC2 State 2X TDM 12 Wide, 4 Banks
LUTs	333	137	370	409
Flops	219	118	158	192
Block RAM	2	0	0	0
Number of Trace Pins	0	13 data (1 bit the clock to view)	12 data + 1 clock	6 data + 1 clock
Timing Results (3.33 ns Constraint)	3.000 ns	1.617 ns	2.839 ns	2.922 ns

Table 1 – Resources required and timing results for various core types at 300 MHz



Figure 5 – EyeScan and EyeFinder view of all bits for 2x TDM core at 300 MHz

Differential or Single-Ended Probing Options

Designers should consider what kind of probing to use for logic analyzer measurements. Some major options include single-ended or differential flying leads, Mictor

connectors, Samtec connectors, or connector-less probes. Concurrent with this decision, you must determine whether to route debugging signals for logic analysis in a single-ended or differential fashion. The deci-

sion rests on clock and data rates and signal integrity for the board layout, and simulating those effects helps to make a decision. In the ATC2 examples, 1.5 Gbps single-ended SoftTouch connector-less probes were used, as shown in Figure 7.

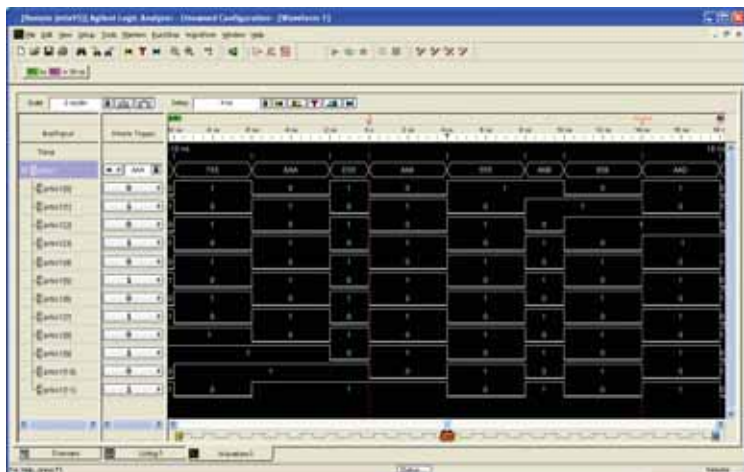


Figure 6 – 300-MHz state capture of 12 data bits from 7 FPGA pins (6 data, 1 clock)



Figure 7 – Single-ended 1.5 Gbps SoftTouch connector-less probe connection to a Virtex-5 FPGA with ATC2 TDM core

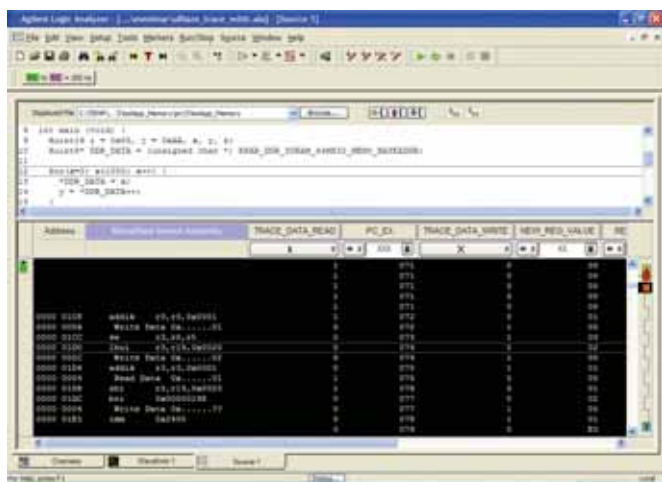


Figure 8 – MicroBlaze 5.0 core inverse assembly and source correlation

MicroBlaze 5.0 Core Trace and Debugging

The embedded MicroBlaze processor cores certainly will be popular in Virtex-5 applications. With the change in architecture for Virtex-5 devices, a new core was required – thus the MicroBlaze 5.0 core. The ability to take an ATC2 state core with the pin compression option, define a single signal bank with key MicroBlaze signals, and offer the user a GUI to fine-tune the signal bank definition is exactly what the MicroBlaze trace core for Virtex-5 devices does. With as few as 16 pins, inverse assembly is possible.

The logic analyzer takes the captured trace from the MicroBlaze core and performs inverse assembly and source correlation to provide a view of program flow as well as data manipulation, as shown in Figure 8. Probing behind the cache simplifies capture so that operations actually performed by the microprocessor are what you see. This trace can also be easily time-correlated to other measurements taken in the digital system, unlocking the power of the logic analyzer for system-level measurements that includes internal FPGA nets, MicroBlaze execution, and external system measurements.

Conclusion

Designers of digital systems with Virtex-5 FPGAs have some powerful options when it comes to probing internal as well as external FPGA signals. There are trade-offs involved with these choices that tie back into pins available, use of block RAM, desired memory depth of capture, and ultimately timing margins.

Overall, measurement cores for logic analyzers provide a practical, time-saving approach to debugging and validation. For those with an embedded MicroBlaze processor, a new measurement core simplifies the process of tracing out program flow without having to worry that caching or pipelining will compromise visibility. For more information, go to www.agilent.com/find/logic or www.agilent.com/find/xilinxfpga.