

# Serial Everywhere — The Triple-Play Challenge

Xilinx is helping to empower the next innovation in the triple-play race.



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The electronics industry is pressed to its limits as it strives to develop solutions to feed the insatiable appetites of the consumer and enterprise markets for voice, video, and computer data communications on a single network. To the global broadcast and telecommunications industries, the triple-play opportunity is at once a potentially inexhaustible source of revenue and a constant source of frustration. Despite the immeasurable reward for successfully delivering triple-play services to the masses, substantial obstacles continue to impede access.

Perhaps the most central of these obstacles is the inadequacy of legacy infrastructure equipment to support the massive increases in bandwidth. Evolving from voice-only, the legacy infrastructure is a complex web of overlaid networks that represents both a financial and technological burden to service providers. In short, it is neither technologically feasible to deliver triple-play services with existing equipment nor economically practical to replace it with a completely new network. Moreover, legacy customers will not tolerate any inter-

ruption of existing services, nor will they pay extra for poor service quality.

Motivated by the promise of substantial rewards to those that enable this massive business food chain, the electronics industry is marshaling every possible resource to find solutions at all levels to the triple-play challenge. It is no surprise that the semiconductor industry endeavors to keep pace with system manufacturers.

## **Xilinx Serial I/O Solutions: Crossing the Chasm**

The evolution of serial I/O solutions in Xilinx® FPGAs is the result of our high-speed serial initiative, which we announced in 2002. The aim of the initiative was (and is) to accelerate the industry's move from parallel to high-speed serial I/O by delivering a new generation of connectivity solutions for system designs that meet bandwidth requirements from 3.125 Gbps to 10 Gbps and beyond.

We began by adding up to twenty-four 3.125 Gbps serial transceivers in our Virtex™-II Pro family, accompanied by IP soft cores for numerous serial connectivity standards, reference designs, hardware development platforms, design software, characterization data, and an in-depth design support program.

The Virtex-4 FX family followed suit in 2005 with a similar complement of broad-range transceivers, this time delivering 622 Mbps to 6.5 Gbps performance, as well as an equally robust set of IP

and design support software, hardware, and services.

In each case, one of the key objectives in the introduction strategy of these products — with their attending high-speed serial I/O solution packages — was to reach the early adopters and innovators within the FPGA customer base with a viable alternative to custom ASIC and ASSP serial I/O solutions.

Having successfully proven the viability of FPGA-based serial I/O solutions with these previous product families, there remained a single yet extremely important evolutionary step. To cross the chasm into the mainstream FPGA customer base and truly create equivalency between Xilinx serial I/O solutions and custom solutions required the delivery of fully verified, fully integrated, hard IP-based, turnkey serial I/O solutions.

With our newest 65-nm Virtex-5 LXT platform, we believe that we have indeed crossed the chasm. By offering the industry's first FPGA to deliver hard-coded PCI Express Endpoint and tri-mode Ethernet media access controller (MAC) blocks, Virtex-5 LXT devices are addressing the bandwidth, power, and cost challenges facing equipment vendors working to enable the emerging triple-play services market. The Virtex-5 LXT platform is optimized to enable FPGA designers across a wide range of applications to benefit from serial connectivity by delivering a comprehensive, fully compliant protocol solution with the greatest ease of use. ●●●