



# Achieve Higher Performance with Virtex-5 FPGAs

New architectural elements can help you attain higher system-level performance.

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In FPGA system design, maximizing performance requires a balanced mix of performance-efficient components – logic fabric, on-chip memory, DSP, and I/O bandwidth. In this article, I'll explain how you can benefit from Xilinx® Virtex™-5 FPGA building blocks, particularly the new ExpressFabric™ technology, in your quest for higher system-level performance. I will explore key features of the ExpressFabric architecture with examples that quantify the anticipated performance improvements for logic and arithmetic functions. Benchmarks based on actual customer designs will show that Virtex-5 ExpressFabric technology performs on average 30% better than previous-generation Virtex-4 FPGAs.

With the new logic fabric (in which you can implement functions such as counters, adders, and RAM/ROM storage) and available hard IP blocks, memory, and DSP (optimized to operate at clock rates as fast as 550 MHz), the Virtex-5 FPGA is clearly the platform of choice for high-performance designs.

## ExpressFabric Performance

Since the first FPGA was introduced in the mid 1980s, the logic fabric for most FPGAs has been based on the same fundamental four-input look-up table (LUT)

architecture. The Virtex-5 family is the first FPGA platform to offer a true six-input LUT (6-LUT) fabric with fully independent (not shared) inputs (Figure 1). Moving to a 6-LUT fabric architecture provides the 65-nm Virtex-5 FPGA family with the most effective trade-off between critical path delay – the determining factor for logic fabric performance – and die size.

With process technology advancements, interconnect timing delay can account for more than 50% of the critical path delay. Xilinx has developed a new interconnect pattern for Virtex-5 FPGAs to enhance performance by reaching more places in fewer hops. The new pattern increases the number of logic connections achievable within two and three hops. Moreover, a more regular routing pattern makes it easier for Xilinx ISE™ software to find the most optimal routes. All of the interconnect features are transparent to FPGA designers, but will translate to higher overall performance and easier design routability. Essentially, the Virtex-5 pattern provides fast, predictable routing based on distance.

The combination of the new 6-LUT structure and special functions like carry chains, dedicated multiplexers, and flip-flops (along with the unique methods by which these elements are connected) creates unsurpassed performance and efficiency for implementing logic and arithmetic functions.

One example that clearly shows the benefits of the ExpressFabric technology is

a multiplexer (MUX). Implementing a 4:1 MUX requires two four-input LUTs and a MUXF block in the Virtex-4 architecture. The same 4:1 MUX can now be implemented in a Virtex-5 device with a single LUT. Similarly, an 8:1 MUX requires four LUTs and three MUXF blocks in a Virtex-4 FPGA, while the new Virtex-5 architecture requires only two 6-LUTs. The result is better performance and better logic utilization, as shown in Figure 2.

As in previous Xilinx FPGA families, the Virtex-5 Slice L (logic slice) can implement logic functions, registers, and arithmetic functions using the dedicated carry chain. The slightly more complex Slice M (memory slice) adds the capabilities of implementing distributed RAM and shift registers within the LUT (SRL).

Among the various improvements provided by the ExpressFabric architecture, the new carry chain structure delivers substantially higher performance when used to implement arithmetic operations. Its effect on critical path delay is readily seen for several examples listed in Table 1.

Distributed memory functions such as LUT RAM or ROM also benefit in several ways from the larger LUT structure. The new aspect ratio allows a much denser packing of small memory functions leading to significant performance benefits, as depicted in Table 2.

The performance increases provided by the improved logic fabric with its 6-LUT architecture and interconnect structure are substantial, but this is only the beginning.

Most applications require more on-chip RAM than what LUT-based RAM can provide. With the enhanced Virtex-5 block RAM, you can achieve higher on-chip memory performance.

**Block RAM Performance**

With the move to 65 nm, the Virtex-5 block RAM inherited a 10% increase in clocking speed to 550 MHz. However, to achieve the desired performance for most applications today, block RAMs need to be more than just faster. They need to be larger.

The Virtex-5 block RAM has doubled in size to 36 Kb. This larger block size (comprising two 18-Kb memories) will support 72-bit data words in simple dual-port mode, thereby doubling block RAM bandwidth. Moreover, the Virtex-5 FPGA provides dedicated connections to enable you to cascade two adjacent 36-Kb block RAMs together in the block RAM column, thereby implementing a 72-Kb memory running at the maximum 550-MHz rate.

The availability of ever-larger FPGAs has accelerated the trend toward integrating more subsystems into a single device, making more common the necessity of interfacing multiple clock domains. Virtex-5 devices accommodate this by providing integrated logic to simplify the implementation of flexible and efficient FIFOs.

Through this combination of enhancements, the Virtex-5 block RAM delivers more on-chip memory, easier to build FIFOs, and higher bandwidth.

**DSP Performance**

The growing acceptance of FPGAs as a viable solution for high-performance DSP applications is well deserved. Whether as a co-processor or a stand-alone solution for

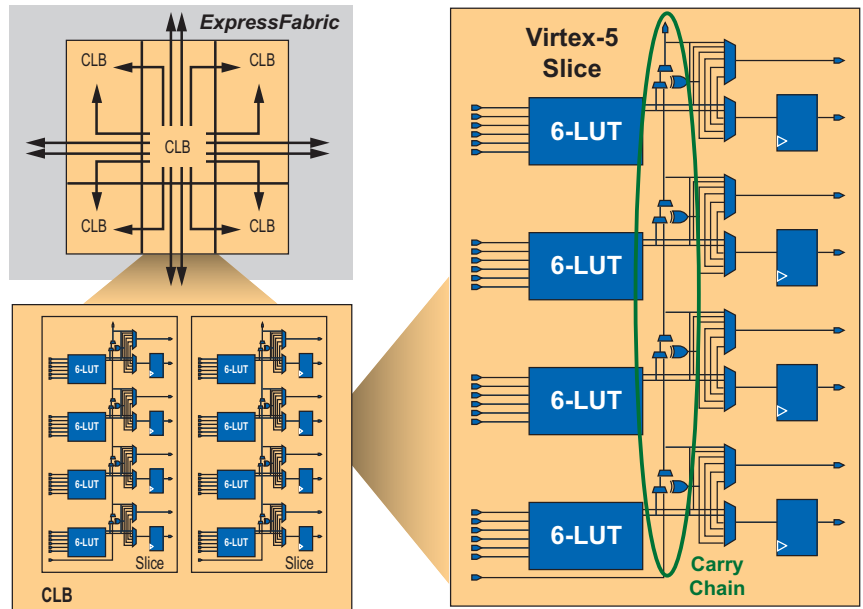
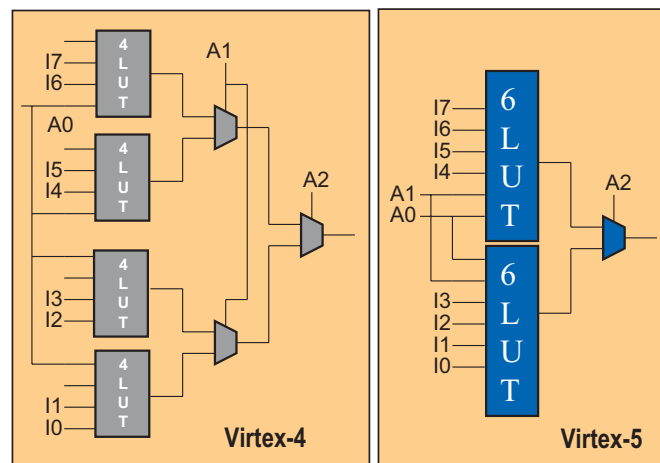


Figure 1 – Virtex-5 configurable logic blocks (CLBs) comprise two slices. Each slice uses four independent 6-LUTs that provide the benefits of fewer logic levels.



8-to-1 MUX	Virtex-4	Virtex-5	Improvement
Logic Levels	2	1	100%
Path Delay	1.33 ns	1.08 ns	23%

Figure 2 – 8:1 multiplexer implemented with Virtex-5 FPGAs versus Virtex-4 FPGAs

Function	Virtex-4 FPGA Path Delay	Virtex-5 FPGA Path Delay	Improvement
Adder 64-bit	3.5 ns	2.4 ns	46%
Ternary Adder 64-bit	4.3 ns	3.0 ns	40%
Barrel Shifter 32-bit	3.8 ns	2.8 ns	37%
Magnitude Comp. 48-bit	2.4 ns	1.8 ns	34%

Table 1 – Arithmetic functions implemented with Virtex-5 FPGAs versus Virtex-4 FPGAs

Function		Virtex-4	Virtex-5	Improvement
LUT RAM 64 x 1	Logic Levels	2	1	100 %
	Path Delay	1.76 ns	1.26 ns	40 %
LUT ROM 128 x 12	Logic Levels	3	1	200 %
	Path Delay	1.84 ns	1.20 ns	53 %

Table 2 – LUT-based RAM/ROM implementations with Virtex-5 FPGAs versus Virtex-4 FPGAs

more demanding applications, FPGAs continue to provide the best combination of performance, power, and cost.

To keep pace with the seemingly insatiable demand for more DSP performance, Xilinx is leading with Virtex-5 DSP capabilities in terms of both clock rate and precision – the clock rate has increased to 550 MHz and the precision has improved from 18 x 18 bits to 25 x 18 bits.

Xilinx also optimized the Virtex-5 DSP48 slice for adder-chain implementations, a powerful capability that enables the creation of very efficient high-performance filters. Dedicated routing resources on the inputs and outputs of each DSP48 slice permit any number of slices to be chained together within a column. This dedicated routing ensures that every DSP48 slice in the chain will run at full speed without consuming any of the fabric routing or logic resources, as other FPGAs require. Taken together, these improvements reduce by half the number of resources needed to implement common high-precision functions. For example, for a 35 x 25-bit multiply, four DSP48 slices are needed with the Virtex-4 FPGA. With the wider DSP block available in the Virtex-5 FPGA, half as many slices are used to implement this multiply function.

**I/O Bandwidth Performance**

As performance benchmarks go, the speed with which an FPGA can process data is relevant only in context with the device’s I/O bandwidth, which is the speed with which large amounts of data can be moved on and off the device. When using external memory buffers, the interface must be at least two times faster than the data-processing rate because data must be both written out of and read back into the FPGA.

Virtex-5 FPGAs improve on Virtex-4 bandwidth by increasing both the data rate per pin and the number of available I/Os with larger packages. For example, for popular memory interfaces like DDR2 SDRAM, the bandwidth has increased per pin from 534 Mbps to 667 Mbps; the number of data I/Os, when considering SSO requirements, has increased from 432 to 576.

blocks generated by CORE Generator™ software (a part of ISE software).

For these benchmarks, we performed synthesis in a timing-driven fashion with Synplicity’s Synplify Pro, using tight, realistic constraints to effectively measure performance. This was done to ensure that all special optimizations and logic replications were employed.

Implementation in ISE software was accomplished with the place and route effort set to high. Clocks were tightened iteratively by 5% increments until the design failed to meet design constraints.

The result was an average performance gain of 30% over designs implemented in Virtex-4 FPGAs, as shown in Figure 3.

Those designs that improved the most have large cones of logic; the critical path implements a large, often complex logic equation. For example, ASIC prototyping designs will typically have very few registers for a large amount of logic in their critical path. These types of designs exhibit a significant improvement with Virtex-5 ExpressFabric technology.

Those designs exhibiting a more moderate improvement either have less levels of logic or provide little opportunity for the use of hard IP blocks or carry-chain structure to improve performance.

Figure 4 summarizes by category the performance improvements of Virtex-5 FPGAs over previous-generation Virtex-4 FPGAs.

**Conclusion**

With its new ExpressFabric technology and tight coupling to other high-performance hard-IP blocks and I/Os, the Virtex-5 FPGA family represents a significant performance boost compared to previous-generation architectures. ●●●

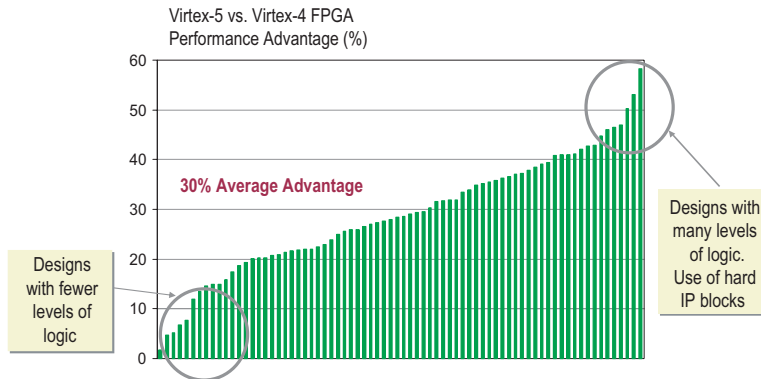


Figure 3 – Comparison based on a suite of 74 customer designs using ISE 8.2i software

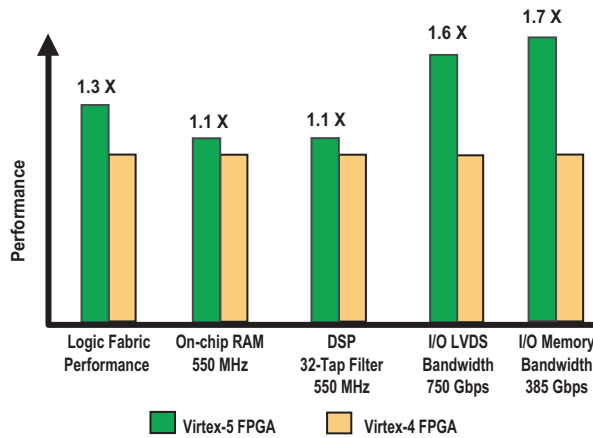


Figure 4 – Virtex-5 FPGA performance improvements

**Customer Design Benchmarks**

To further evaluate the performance improvements provided by the Virtex-5 FPGA logic fabric, we implemented a set of customer designs using Xilinx ISE software.

These designs were all written in VHDL or Verilog. We implemented some specific design units like memories and FIFOs using direct instantiation of library components or synthesis inference, but many were implemented using EDIF