

Getting the Best Results from Virtex-5 FPGAs

Synplicity applies new algorithms and heuristics for optimal Virtex-5 support.

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The revolutionary capabilities of Xilinx® Virtex™-5 devices can be fully realized only if the EDA technologies to unlock those capabilities are available when the device is. To achieve this, the FPGA architecture and corresponding EDA design tools must be developed simultaneously. The scale of EDA development over previous generations is similar to the difference between Virtex-5 devices and their previous generations.

As the first FPGAs created at the 65-nm technology node, the Virtex-5 family of domain-optimized devices provides as much as 65% more logic cells and 25% more I/O pins than the Virtex-4 family. At the same time, devices in the Virtex-5 family provide 30% higher performance, 35% lower dynamic power dissipation, and consume 45% less silicon real estate when compared to their Virtex-4 counterparts.

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Clearly, the Virtex-5 architecture delivers revolutionary capabilities. To develop a synthesis flow that leverages these new features, Xilinx gave Synplicity early access to the Virtex-5 architecture. By the time the first Virtex-5 devices were introduced, we had been working side-by-side with Xilinx engineers for more than a year to enhance our Synplify Pro synthesis engine. This involved making substantial algorithmic changes to Synplify Pro software to maximize the performance and logic density of Virtex-5-based designs. Because of our partnership, we have the tools and methodologies in place to enable you to rapidly deploy these devices.

In this article, I will describe some of the ways in which we enhanced the Synplify Pro FPGA synthesis engine to take full advantage of the capabilities offered by the Virtex-5 family.

New Algorithms to Synthesize 6-LUTs

Increases in the complexity of the FPGA fabric demanded corresponding increases in the sophistication of the synthesis algorithms. If you applied the same algorithms for a fabric based on 4-input look-up tables (4-LUTs) to a fabric with 6-LUTs, for example, synthesis run times would dramatically increase. To take full advantage of the specialized architectural features in the Virtex-5 family, Synplicity had to either fine-tune or in some cases completely re-craft the underlying synthesis algorithms.

To reduce the levels of logic needed to map functions like wide data paths and DSP, the ExpressFabric™ technology in the Virtex-5 family features LUTs with six independent inputs (Figure 1). This significantly reduces the number of logic levels and LUT area required to implement wide functions. Within the synthesis process, you can use each of these logical elements as a true 6-LUT or as two 5-LUTs that share their five inputs.

However, the combinatorial explosion associated with mapping to 6-LUTs can cause memory utilization and run-time problems if not handled correctly. If you applied the algorithms for a fabric based on 4-LUTs to a fabric with 6-LUTs without significant modification, synthesis run times would be orders of magnitude longer (if they completed at all). In addition, when attempting to find an optimal mapping, traditional algorithms run the risk of becoming trapped in local minima.

Unlike timing-driven engines, most conventional synthesis engines simply attempt to reduce the number of logic levels. This is problematic for LUT architectures in which different input-to-output paths have asymmetric delays. Consider the five shared input pins versus the sixth unique pin in Figure 1; these pins will have very different delays.

The fact that you can use Virtex-5 LUTs in a 2 x 5-input configuration further increases the complexity of the mapping operations. Synthesis tool vendors must conduct a lot of research and development to use structures that share inputs but represent different functions.

Synplicity equipped Synplify Pro software (which features a unique direct-mapping capability) with a variety of sophisticated heuristic algorithms that are tailored to minimize the number of cuts, handle huge capacities, and address these complex mapping and timing scenarios.

Timing Estimation with Diagonally Symmetric Interconnect

Another ExpressFabric feature is a radically new form of diagonally symmetric interconnect that reaches more locations with fewer hops (Figure 2). This diagonally symmetric interconnect pattern was designed to improve speed and predictability. The combination of ExpressFabric 6-LUTs and a diagonally symmetric interconnect pattern results in an average increase of logic performance of 30% over Virtex-4 devices, which equals two speed grades.

The diagonally symmetric interconnect pattern also delivers significantly higher complexity in timing analysis; previous physical synthesis algorithms were based on architectures with “Manhattan routing” or 90-degree routes. To handle the

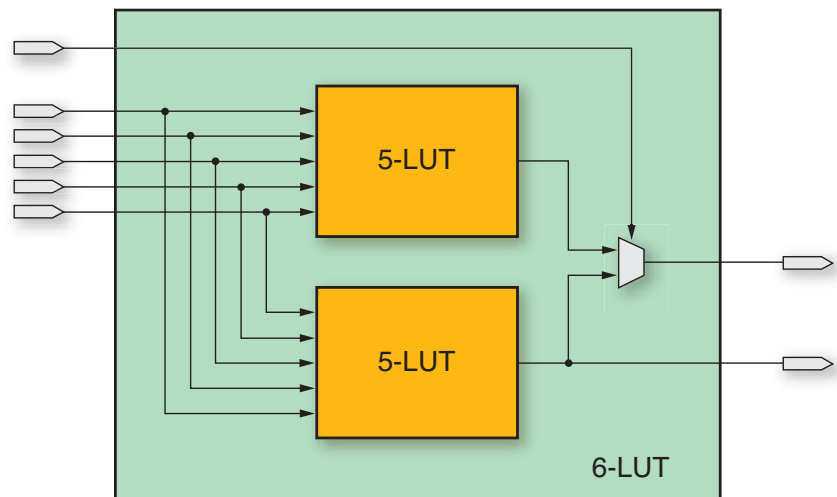


Figure 1 – Virtex-5 six-input LUTs

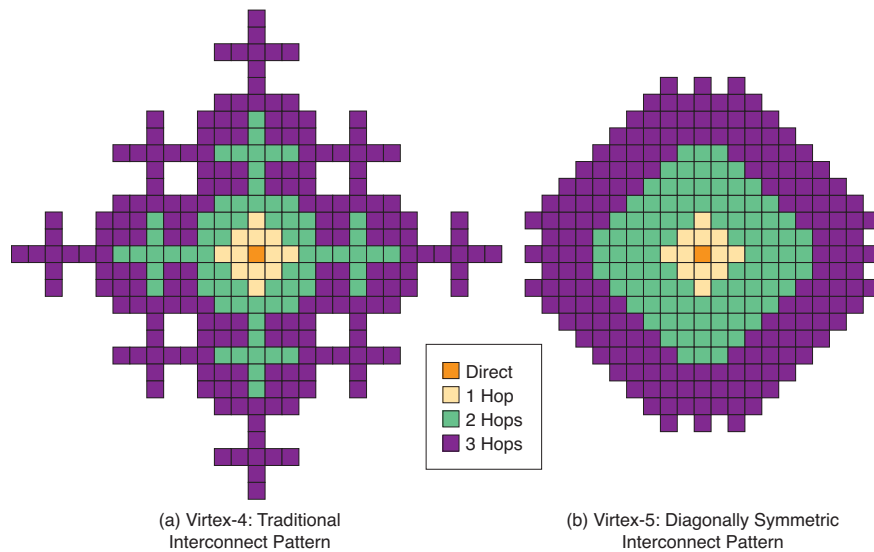


Figure 2 – Diagonally symmetric interconnect routing

combination of both 90-degree and diagonal routes, Synplicity custom-designed new algorithms and delay models. As opposed to simple wire-load models, we engineered the Synplify Pro tool to employ sophisticated netlist-based routing estimation (coupled with known routing values where applicable). In the case of fast carry chains, for example, routing delays are well known and can be directly “plugged in.” Similarly, in the case where a cell, driver, load, and specific route are known, an accurate routing delay associated with this path can be plugged in to the routing and timing algorithms.

Synthesizing Fast High-Capacity RAM Blocks

The new block RAM structures (with pipeline) in the Virtex-5 family have increased to 32 Kb in size – twice the size of those found in Virtex-4 components. In addition to offering a simple dual-port mode that can double the RAM’s bandwidth, these blocks also contain additional hard IP in the form of FIFO logic and new 64-bit error checking and correction (ECC) logic (Figure 3). Implementing this logic as hard IP frees up other resources and minimizes dynamic power consumption.

As with all hard IP blocks in Virtex-5 devices, these block RAMs have been

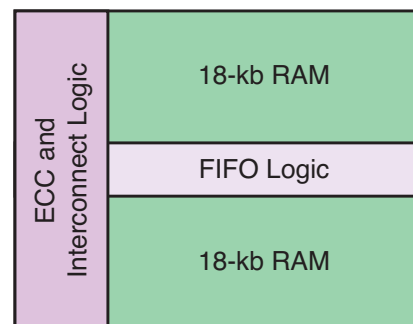


Figure 3 – The Virtex-5 family features as much as 10 Mb of 550-MHz block RAM.

tuned for 550-MHz operation to provide higher on-chip memory bandwidth. The 18-Kb block RAMs are constructed from two physical 9-Kb memories, which are automatically controlled to save power by enabling only one of the 9-Kb sub-blocks for any given read or write operation in most configurations.

For our part, the Synplify Pro synthesis software can perform automatic memory inferencing, including single-port and dual-port implementations, single and multiple clocking schemes, and automatic retiming. Regarding the latter point, Virtex-5 block RAMs are inherently synchronous; however, the design’s RTL could describe the memory and registers in such a way as to be technically asynchronous. In such a case,

the Synplify Pro tool has the ability to “push” the registers into the RAM.

Similarly, the software will recognize potential conflicts and automatically generate appropriate conflict-resolution logic. In cases such as dual-port RAMs, for example, in which the result of writing two words to the same address may be undefined, the Synplify Pro tool automatically inserts the appropriate logic to resolve the issue such that the memory works in exactly the same way as the RTL will simulate.

Furthermore, Synplify Pro software can automatically analyze the memory described in the design and recognize potential issues in mapping it to preferred memory resources. If you require block RAM, for example, but have used more than what is available on the physical device, the software will automatically move some of the memory into select RAM.

Optimal Use of Faster, Wider DSP Blocks

The Virtex-5 hard DSP slice – called the DSP48E – features a 25 x 18-bit multiplier (versus the 18 x 18-bit multiplier employed in Virtex-4 FPGAs). This increase can lead to fewer cascaded stages, thereby resulting in higher overall performance and utilization (Figure 4).

Tuned for 550-MHz operation, you can configure these high-precision, high-performance, highly flexible slices for DSP, arithmetic, and logic functions and cascade them for adder-chain architectures. The DSP48E slice has 40% lower power consumption compared to equivalent functions in Virtex-4 FPGAs (1.38 mW/100 MHz at a 38% toggle rate).

The sophistication of these DSP slices means that it is unlikely that a data path defined in RTL will exactly match the optimal DSP implementation structure. For example, rather than implementing a function such as “(a + b) + (c + d)” by adding “a” and “b,” adding “c” and “d,” and then adding the results generated by these operations, it may be more efficient to cascade the DSP slices along the lines of “(((a + b) + c) + d).”

We equipped Synplify Pro software with extremely sophisticated mapping algorithms that perform a lot of data path massaging, creating data path structures that

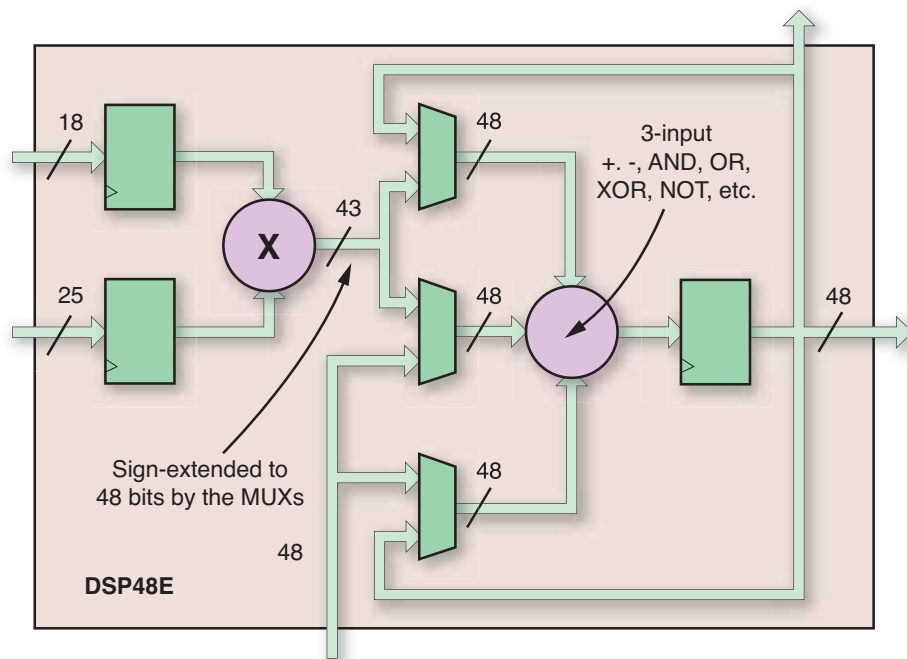


Figure 4 – Virtex-5 DSP slices with 25 x 18 multipliers

map efficiently onto – and take full advantage of – the DSP48E slices featured in Virtex-5 SXT devices.

Note that the DSP48E slice contains a large number of registers (not shown in Figure 4 for simplicity). The Synplify Pro tool can use advanced pipelining and retiming techniques to take full advantage of these embedded register elements. Another consideration is that these internal register elements support only synchronous resets. Thus, if you employ an asynchronous reset in your code, the Synplify Pro tool automatically inserts the appropriate glue logic to restore the required functionality.

Synthesis Considerations with High-Speed I/Os

The number and type of available I/O in a specific device plays a critical role in design implementation, particularly when the application of the FPGA is chip- or system-level verification. With Synplicity tools like Certify ASIC RTL prototyping and the Synplify Pro synthesis solution, we optimized the powerful I/O capabilities in Virtex-5 devices to take into account both signal integration as well as automatic I/O assignments.

Virtex-5 FPGAs offer as many as 1,200 general-purpose input/output (GPIO) pins that you can use to implement industry-

standard and custom protocols. The SelectIO™ technology behind these pins provides 1.25 Gbps differential I/O and 800 Mbps single-ended I/O.

Second-generation ChipSync™ source-synchronous technology allows programmable delays to be individually applied to each input and each output. Furthermore, the unique power and ground pin pattern of the Virtex-5 second-generation sparse chevron packaging technology simplifies circuit board layout while minimizing signal integrity and crosstalk effects. Combined, these I/O technologies ensure reliable operation for high-bandwidth interfaces such as DDR2 and QDR II.

We engineered Synplify Pro synthesis software to automatically handle differential signals (and bi-directional I/O signals). For example, if you apply an attribute that identifies the port as being a low voltage differential signal (LVDS) output port, the Synplify Pro tool will automatically insert the appropriate LVDS primitive with one input and two outputs.

Next Steps

As devices move deeper into the submicron domain, the symbiosis between FPGA vendors and EDA vendors increases. Working

with engineers at Xilinx for almost a year to enhance our Synplify Pro synthesis engine has yielded tremendous benefits, including having the best synthesis technology available immediately when the device was brought to market, tested against real designs.

Future FPGA platforms will provide even greater densities and capabilities, further expanding the reach of advanced FPGA architectures across a wide range of application domains. These new platforms will require ever-more-sophisticated design flows and synthesis solutions. For this reason, Synplicity and Xilinx formed an Ultra-High-Capacity Timing Closure Task Force. As part of this endeavor, engineering teams from both of our companies will collaborate to define and implement new design flows that maximize design productivity and quality of results for ultra-high-density designs implemented using next-generation FPGAs.

The task force will initially focus on dramatically improving overall quality of results and run times, and ensure the stability of results when small changes are made to designs. Ultimately, the goal of the task force is for designers to realize the benefits of near push-button results for ultra-high-density designs, completing multiple design iterations per day.

Conclusion

The Virtex-5 family from Xilinx has an implementation flow engineered by Xilinx and Synplicity to achieve the best possible results. These new FPGAs boast a wide range of new architectural features, such as 6-LUTs and a diagonally symmetric interconnect fabric.

The matching software solution from Synplicity features new forms of timing estimation for diagonal interconnect, new synthesis algorithms to deal with combinatorial explosion, specialized RAM inferencing and I/O handling, and numerous improvements that enable stable results with minor design changes. Taken together, Virtex-5 devices and Synplify Pro software bring system designers new capabilities that you can design with today. ●●●