

Clock Management in Virtex-5 Devices

Virtex-5 FPGAs give designers fresh choices.

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As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance; managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices.

Traditionally, you would deploy solutions such as a Xilinx® Virtex™-4 digital clock management (DCM) or mixed-signal phase-locked loop (PLL) to achieve clock tree deskew and frequency synthesis, among other functions. Yet each solution has its advantages and disadvantages.

In Virtex-5 devices, for the first time in an FPGA, both digital DCMs and analog PLLs are implemented side by side in a clock management tile (CMT). You can now select the clock management solution best suited for your particular applications.

Each Virtex-5 device has as many as six CMTs. A CMT contains two DCMs and one PLL. You can use either of the two DCMs or the PLL as a stand-alone module, or they can interact with each other. If used as a stand-alone module, the application requirements typically dictate which clock management solution to use. The DCM, for example, supports a fine phase shift, a dynamic phase shift, and a multi-

ply/divide feature that does not depend on any maximum VCO frequency. However, the PLL filters input clock jitter, support a wide range of output frequencies with higher frequencies, and consume less power.

The DCM and PLL are also designed to interact with each other. The PLL can help clean up input or output clocks to the DCM. Dedicated resources within each CMT make the connections and still guarantee a proper deskew of the FPGA clocks. The CMTs are located in the center column of the Virtex-5 architecture. This enables well-matched clock routes to and from every DCM or PLL for enhanced symmetry (see Figure 1).

DCM

Virtex-5 DCMs provide a zero propagation delay buffer, clock division and multiplication capabilities, fixed and dynamic fine phase shift, and multiple phases of the input clock. Along with fully differential global clock trees and low skew between output signals, the application's various clocks are distributed efficiently throughout the device. Each DCM can drive as many as 9 of the 32 global clock routing networks within the device.

The global clock distribution network minimizes skews caused by loading differences. By monitoring a sample of the DCM output clock, the DLL compensates

for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DCM provides multiple phases of the source clock. The DLL can also act as a clock doubler or divide the user source clock by as much as 16. The DCM can also act as a clock mirror. By driving the DCM output off-chip and then back in again, the DCM can deskew a board-level clock between multiple devices.

Another submodule provides the ability to phase shift the DCM's output clock in small increments (1/256th of the period). The versatile digital phase shift (DPS) operates in four different modes for maximum flexibility: fixed, variable-positive, variable-center, and direct. The DCM's digital frequency synthesis (DFS) module provides two outputs, CLKFX and CLKFX180, which are derived from the input clock by frequency multiplication and division. You provide valid multiply (M) and divide (D) values, which the DFS implements through a frequency calculator. For example, if you provide an M value of 19 and a D value of 8, they would yield a 2.375 source-clock multiplier.

PLL

The CMT's PLL is a mixed signal block designed to support clock network deskew,

frequency synthesis, and jitter reduction. The PLL block diagram in Figure 2 provides a general overview of the various components.

Input multiplexers (MUXs) are used to select the reference and feedback clocks from the global clock pins, global clock trees, or one of the DCMs. Each clock input has a programmable counter. This pre-scales the reference clock and allows a wide range of frequency synthesis.

The phase frequency detector (PFD) compares both phase and frequency of the input clock and the feedback clock. A signal is generated that is proportional to the phase and frequency error between the two clocks, which is then used to drive the charge pump and loop filter to generate a reference voltage to the VCO. An up or down signal from the PFD determines if the VCO should operate at a higher or lower frequency.

After the PFD determines that the input and feedback clocks are phase- and frequency-aligned, a lock signal is raised, indicating that the PLL output clocks are valid. The VCO continues to compensate for any variations in voltage or temperature. The M counter in the feedback path controls the feedback clock and multiplies the VCO frequency to the desired target frequency. The VCO output clock drives six output counters. Each can be independently programmed to generate a variety of frequencies for the application design.

Additionally, clock switchover, phase shifting, various duty cycles, and bandwidth control are also supported. You can dynamically select one of two input clocks before or during operation. In many cases, alternate phases of a clock are required. The VCO provides eight phase-shifted clocks at 45 degrees each. The higher the VCO frequency, the smaller the phase-shift resolution of the clocks coming out of the 0 counter.

You can individually program each output counter to provide a separately phase-shifted clock. The PLL can also generate non-50/50 discrete duty cycles in each output counter. The resolution and possible output duty cycles depend on the divide value. The higher the output divide value, the higher the resolution setting of the output duty cycle.

Conclusion

Virtex-5 FPGAs give digital designers a choice of either digital or analog clock management. Depending on your particular application, either module – or a combination of both modules – provides you with choices that you never had before.

Together with an abundance of clock tree resources, Virtex-5 devices greatly sim-

plify and improve system-level designs involving high fan-out and high-performance clocks. Virtex-5 devices have powerful frequency synthesis, phase-shifting, and clock deskew capabilities never offered before in an FPGA. Along with comprehensive software support, you can achieve larger, faster, and more complex designs than in any previous-generation FPGA. ●●●

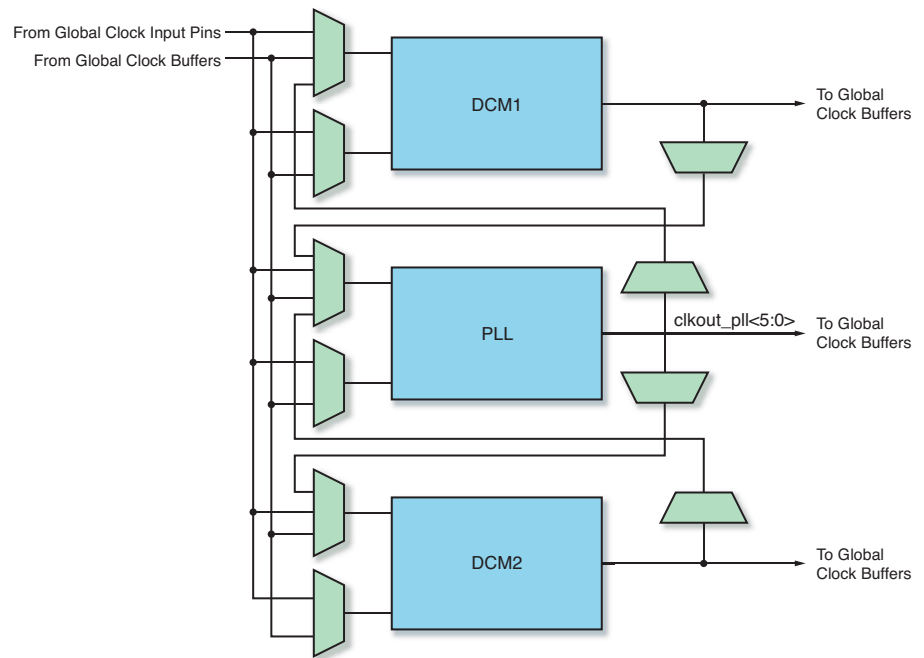


Figure 1 – Virtex-5 CMT block diagram

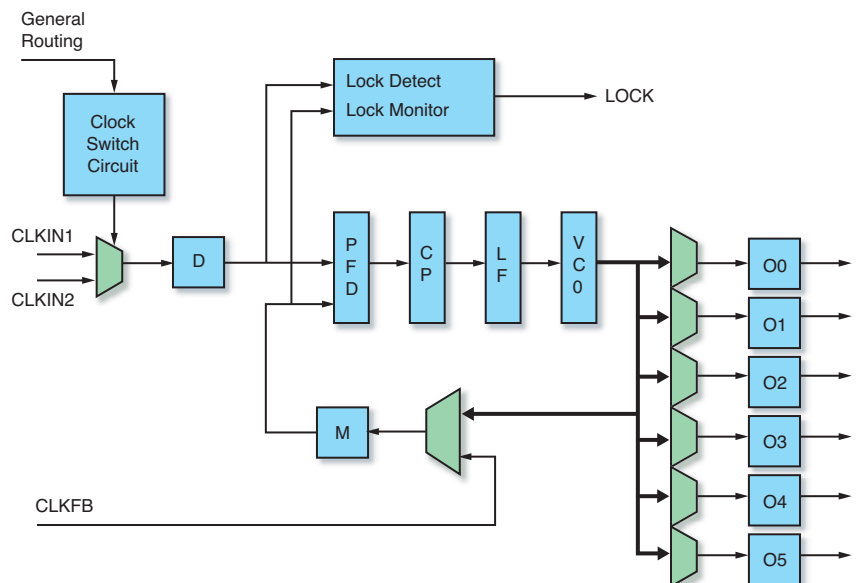


Figure 2 – PLL block diagram