



# Applying Compact Thermal Models

Xilinx gives you one more tool in the FPGA thermal management toolbox.

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Although Xilinx has made substantial progress at the silicon level to reduce static and dynamic power in FPGAs, each successive family takes advantage of reduced feature sizes to increase transistor density and performance – thus resulting in thermal concerns for the top end of the family. You should not underestimate the importance of power consumption mitigation for these devices.

Designers cannot afford inaccurate temperature predictions when power consumption is high and thermal budget margins are low. Flip-chip packages used in high-performance FPGAs have multiple heat-flow paths and are thermally efficient. Using the basic “one-resistor” figure of merit thermal resistance –  $\Theta_{ja}$  – in estimating temperature does not do justice to the thermal efficiency of the packages.

Thus, a need exists for an alternate and more accurate approach to obtain  $T_j$  predictions on these components in an end-user’s environment. This is where the boundary condition-independent compact thermal model (BCI-CTM) becomes useful. You can conveniently use these models to make faster and more accurate  $T_j$  predictions.

In this article, I’ll discuss better ways to predict temperature for these faster and denser FPGA components in a system environment. I’ll also introduce the availability of and support for compact thermal models for Virtex™-4 and Virtex-5 devices as one way to help system designers and component selectors estimate temperatures in the pre-design and implementation phases.

### Motivation for Better Predictive Models

In a specific system implementation, the actual component  $T_j$  may be different from the arithmetic predictions using the published  $\Theta_{ja}$ . The prediction depends on the environment and the prevailing conditions in the system. The following equation governs the relationship:

$$\Theta_{ja} = \frac{T_j - T_a}{P}$$

Or, stated in  $T_j$  prediction form:

$$T_j = T_a + P * \Theta_{ja}$$

where

$\Theta_{ja}$  is the thermal resistance between the device junction and ambient

$T_j$  = junction temperature of the device

$T_a$  = ambient temperature

$P$  = package power dissipation

Although you can easily determine  $T_j$ ,  $T_a$ , and  $P$ , representing the thermal resistance in an application is not easy, particularly for packages with multiple thermal paths. The single parameter  $\Theta_{ja}$  is strongly influenced by the application environment and therefore does not represent a suitable thermal resistance.

### Theta-ja – The Misunderstood Model

Theta-ja has become the base thermal parameter most engineers gravitate toward when estimating component  $T_j$  with known  $T_a$ . But for a more demanding, higher wattage component on a large multilayer system board – particularly with other components around it – this approach often leads to an erroneous prediction of  $T_j$ .

In a design with loose margins in the thermal budget, the simple prediction using published  $\Theta_{ja}$  data may not be an issue. Indeed, it will likely lead to a system running at a lower than predicted  $T_j$ , because most common board types are more efficient than the largest standardized thermal board. Increasingly, with higher wattage components where margins are tight, “conservative” data may be the difference between selection and rejection of the component in a specific program.

The key point here is that  $\Theta_{ja}$  was not meant to be used in these types of predictions. JEDEC, the semiconductor engineer-

ing standardization body of the Electronic Industries Alliance, explains in EIA/JESD51-2 that “the intent of Theta-ja measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.”

A typical implementation of a one-cubic-foot  $\Theta_{ja}$  still-air standardized environment is depicted in Figure 1. This is

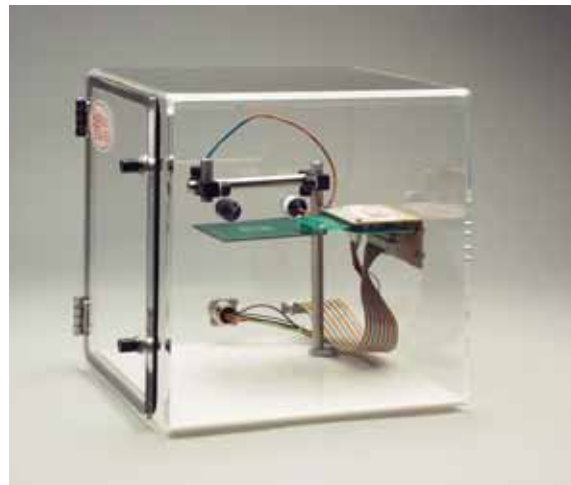


Figure 1 – The Analysis Tech implementation of Theta-ja standardized environment

is 10.8° C per Watt. Although the  $T_j$  prediction expression will suggest a 43.2° C above ambient for 4W dissipation, actual detailed simulation shows a much lower number – and thus suggests a lower effective  $\Theta_{ja}$  – of close to 5° C per Watt.

Table 1 shows the corresponding  $T_j$  for the same component dissipating 4W on various FR4 board sizes and layer counts. This illustrates the power of the environment or boundary conditions on the effective  $\Theta_{ja}$ , and the type of  $T_j$  prediction discrepancy that can result.

Note that while in general the effective  $\Theta_{ja}$  tends to be lower on larger board environments, it can also trend higher and under-predict  $T_j$  on small cards in confined places like PDAs or cell phones. The same rationale is at play –  $\Theta_{ja}$  is not boundary condition-independent. A component with  $\Theta_{ja} = 22^\circ$  C per Watt on a JEDEC board can easily exhibit a 30° C per Watt-effective  $\Theta_{ja}$  on a 30 mm x 30 mm card.

Some application engineers have suggested that because most high-performance devices use denser and larger PC boards,

Xilinx 35 x 35mm FF1136-5VLX50T*		Board Size		
		4" x 4" Board	10" x 10" Board	20" x 20" Board
Layer Count of Mounted Board**	4	68.2° C	64.3° C	-
	8	63.0° C	50.9° C	48.3° C
	12	60.4° C	47.0° C	45.7° C
	16	59.1° C	46.6° C	44.9° C
	24	-	45.3° C	44.0° C

\* Single component considered at 25° C ambient

\*\*All layers have 1 oz Cu with 80% coverage except outer layers that have 2 oz with 20% coverage.

Table 1 –  $T_j$  matrix for FF1136-XC5VLX50T on various boards

clearly not a typical system environment. Ideally, you should use these numbers to compare package efficiency, reserving any serious  $T_j$  prediction for other tools using models that are more relevant.

To illustrate the pitfalls and potential discrepancies in  $T_j$  predictions, let's look at a Virtex-5 flip-chip component – XC5VLX50T- FF1136. The published  $\Theta_{ja}$

component suppliers should provide  $\Theta_{ja}$  using a larger “JEDEC/network board” – a board that may be closer to network application boards. This seems like a good argument and should be advocated at the next JEDEC forum. However, regardless of the board used for data gathering, the prediction will be wrong for some applications. Additional JEDEC boards and standard-

ized enclosures will only lead to more flavors of  $\Theta_{ja}$ , further confusing the issue. There ought to be a better way.

**What Should an Engineer Do?**

Engineers should view  $\Theta_{ja}$  with caution when predicting  $T_j$  in specific environments. Xilinx will continue to publish  $\Theta_{ja}$  and other thermal resistance data because those are the prevailing standards. They have their uses and should be deployed with their limitations in mind.

To address these limitations and to make more accurate  $T_j$  predictions in a system environment, a more refined model of the package is needed. Recognizing this need, Xilinx now supports compact thermal model data for high-performance FPGA devices.

**What is a Compact Thermal Model?**

A compact thermal model is a behavioral model that seeks to accurately predict the temperature of the package at selected nodes: junction, case, top, bottom, and balls, for example. It cannot predict the temperature at any other part of the package that is not predefined. It can be viewed as a reduced node abstraction of the response of a component to various boundary conditions. It is also more computationally efficient than the corresponding detailed model. These models are supplied for use in compatible computational fluid dynamics (CFD) tools for thermal simulations in place of detail models.

Xilinx offers two model types for FPGA products:

1. Two-resistor (2-R) compact models comprising the familiar Theta-jc and Theta-jb for the package. There is no geometrical information. Although 2-R models are useful and give better predictions than traditional  $\Theta_{ja}$  estimations, they are not as accurate as Delphi models.
2. A Delphi compact model comprising several thermal resistors that connect a junction node (representing the die) to several surface nodes. Thermal links are also allowed between the surface nodes. Figure 2 shows the topology for a flip-chip BGA Delphi compact model. The matrix of resistors has been optimized through a Delphi optimization algorithm so that they can be used in various environments without compromising prediction accuracy.

Table 2 depicts a typical Delphi half-matrix model for flip chip. The resistance data is usually saved along with the node definitions and package extents to complete the model.

JEDEC has proposed a neutral file format in XML for CTM distribution. Xilinx plans to support the format when CFD tools adopt and support it. In the interim, Xilinx is offering the CTM files in two CFD tool formats, Flotherm and Icepak, selected from a pre-introductory survey of Xilinx customers. These tools cover the majority of those end-users who answered the survey. If you do not use one of these tools, you can request ASCII data for manual or script-based entry into your tool.

**Application Examples**

Figure 3 shows a typical flow for a CTM application. Normally, the component CTM data is stored in a library; as the user, you will bring in the CTM data as a library item. You then specify the board attributes and boundary conditions of your assembly, adding other items like component power and heat contributions from other components for the  $T_j$  prediction.

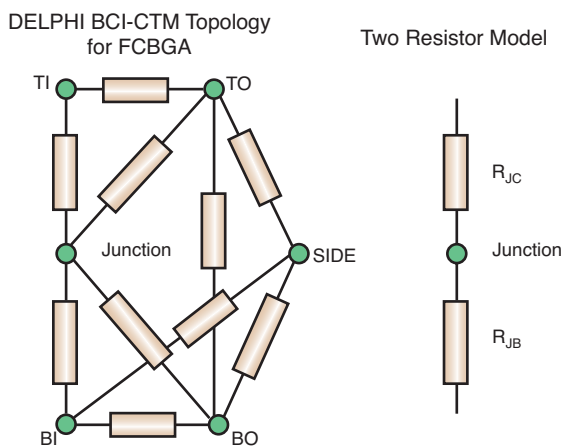


Figure 2 – CTM topologies

**Schematic Overview  
CTM Implementation Concept**

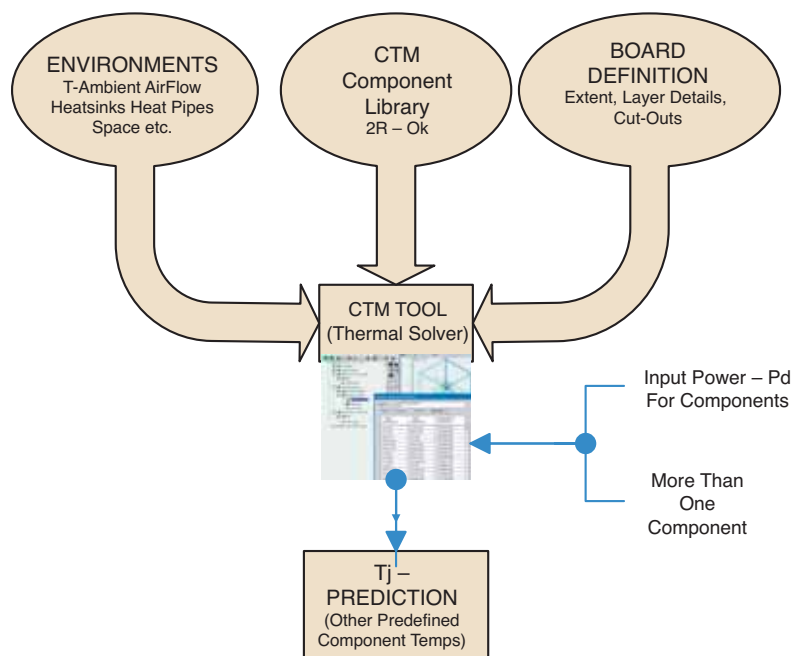


Figure 3 – CTM application schematics

Delphi Compact Model (C/Watt)	Top Inner (TI)	Bottom Inner (BI)	Top Outer (TO)	Bottom Outer (BO)	Side
Junction	0.22	1.25	1.05	14.97	-
Top Inner (TI)		16.14	4.45	-	-
Bottom Inner (BI)			-	9.47	11.1
Top Outer (TO)				14.55	3.18
Bottom Outer (BO)					4.72

Table 2 – Delphi CTM resistors for FF676-XC5VLX50

Let's examine the benefits of CTM prediction in the cases below.

#### Case Study #1:

##### Battleboard Temperature Estimations

The "battleboard" is a 24-layer 20 x 16-inch board that Xilinx uses to assess signal integrity issues on Virtex components. In this case, lab measurements showed that a Virtex-4 component case temperature was well below what you would expect from the  $\Theta_{ja}$  prediction. A discrepancy of about 20° C was apparent. The Icepak CFD model using CTM inputs with radiation "on" showed a more realistic  $T_j$  – very comparable to those measured in the lab. Table 3 summarizes the observations (note that reported temperature is T-case).

#### Case Study #2:

##### Small Board with Multiple Components

A 3.75 x 2-inch board can illustrate the small board size effect and the influence of adjacent components on the  $T_j$  prediction of the component of interest. I have used the BCI-CTM approach with the aggressor components in active and inactive states to show the impact on  $T_j$  prediction.

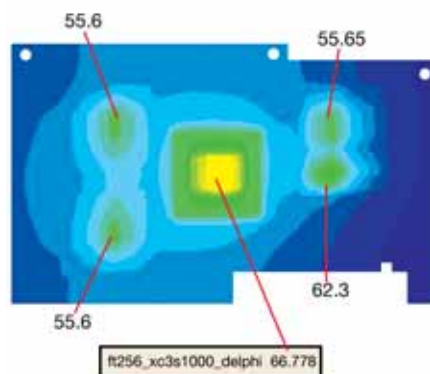


Figure 4 – Contours of static temperature

The high-density interconnect (HDI) board used in this case is smaller than the JEDEC standard 2S2P board. The Xilinx XC3S1000-FT256 component deployed on this board has a  $\Theta_{ja}$  of 19.7° C per Watt. With a 20° C ambient, and without any board input, you can predict a  $T_j$  of 39.7° C ( $20 + Pd * \Theta_{ja}$  [100LFM]).

The BCI-CTM model with 100 linear-feet-per-minute (LFM) airflow shows a  $T_j$  of 55° C with  $T_a = 20°$  C for

the single component on the board. The predicted  $T_j$  is already worse than the JEDEC prediction. This case is in line with what you would see with smaller components that use smaller, thinner boards in consumer products – PDAs, MP3 players, or GPS systems.

Figure 4 shows the board temperature contour with four chip-size package (CSP) components doing 0.25W each. The 8-mm-square CSP components used 2-R data (published jb and jc) in the model. Figure 4 shows the component temperatures. The XC3S1000-FT256 component yielded a  $T_j$  of 65° C – a further 10° C rise over the single component case. Both single and multi-component runs took less than four minutes on a conduction-based tool using the Delphi CTM for the Xilinx component. These predictions are clearly different from what the basic  $\Theta_{ja}$  parameter predicted.

#### Conclusion

Relying on the basic  $\Theta_{ja}$  metric to predict junction temperature for high-performance devices in a system is inadequate and can cause errors that could lead you to preclude a perfectly good component in your system. To address this shortcoming, Xilinx provides compact thermal models to assist in predicting  $T_j$  – in stand-alone calculations as well as system deployments.

You can use these models in CFD tools to make  $T_j$  predictions that take your environment and board conditions into consideration. Although you can accomplish the same predictions with a detailed package model, note that these CTMs offer reduced node benefits of faster solutions that are also computationally efficient.

You can download Virtex-4 and Virtex-5 CTM data at [www.xilinx.com/xlnx/xil\\_sw\\_updates\\_home.jsp](http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp). Future high-performance FPGA products will have the Delphi models available for download as part of thermal collateral. Xilinx will also support legacy products such as Virtex-II and Virtex-II Pro devices, older Spartan™ FPGAs, and CPLD products on a by-request basis.

Hand Calc	Reported	ICEPAK CFD solution < 4 min	
$T_j - JA = 10.6°$ C/watt (1-R model $T_a = 25°$ C)	Battleboard $T_c$ $T_a = 25 - 27°$ C	$T_j$ ; 2-Resistor Model $T_a = 25°$ C	$T_j$ : Delphi Model as Published ( $T_a = 25°$ C)
		JB = 2.6 and JC = 0.19° C/watt	
67.4° C	46.4° C	48.8° C	43.9° C

Table 3 – "Battleboard" temperature predictions