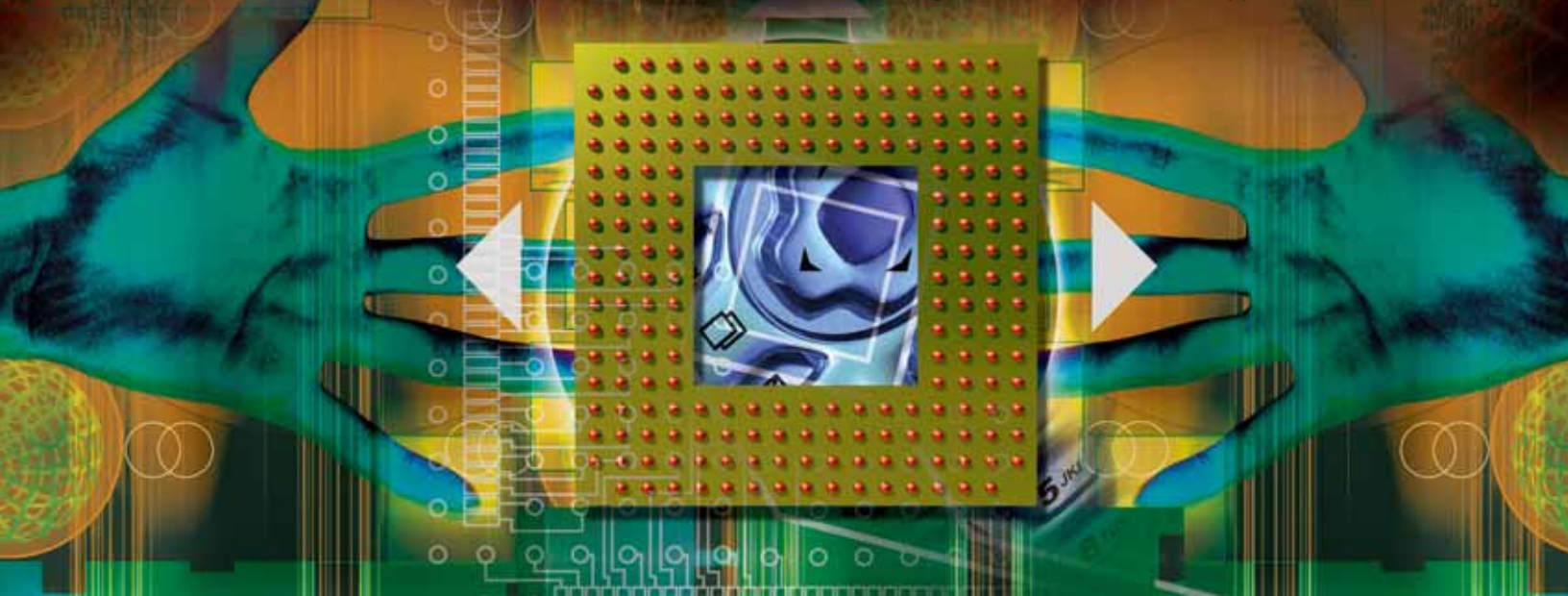


# A Multi-Gigabit Transceiver for the Masses

The Virtex-5 GTP transceiver brings versatility, ease of use, power efficiency, and cost-effectiveness to high-volume mainstream applications.



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The incessant demand for ever-increasing bandwidth has led designers away from parallel buses and low-speed transceivers toward serial transceiver-based interfaces. High-speed signals solve many design challenges; they offer new levels of bandwidth and lower overall system cost and power consumption.

These successes have led engineers to believe that the industry can continue to lower overall cost and power simply by increasing transceiver speed indefinitely. However, going beyond 3 Gbps can in some cases lead to fundamentally different engineering challenges that make it harder to lower overall system cost and power consumption. The explanation is simple; maintaining signal integrity becomes increasingly difficult at ultra-high speeds,

and the extra overhead can sometimes outweigh the benefits associated with increased data rates.

## Transceivers in Transition

Figure 1 shows the frequency loss and crosstalk associated with a legacy backplane channel. At 1.6 GHz, the loss is reasonably manageable, making transceiver implementation at or below 3.2 Gbps relatively cost-effective and power-efficient.

However, at 3 GHz, the loss becomes significant. Consequently, the implementation of a 6 Gbps backplane transceiver requires different feature sets. You will likely need advanced techniques such as decision feedback equalization (DFE) to maintain signal integrity, and these advanced capabilities require a different set of optimized features.

This explains why a 3 Gbps transceiver typically consumes less than 100 mW per channel, whereas a DFE-enabled 6 Gbps transceiver consumes at least twice as

much power. For applications requiring these advanced features, this extra power consumption is a worthwhile trade-off. But it becomes advantageous to offer both a low-power 3.2 Gbps transceiver and a high-performance transceiver for cutting-edge applications – in essence offering the best tool for the job.

At 5 GHz, the signal-to-noise ratio (SNR) becomes negative. In that case, you would have to redesign the entire backplane with more expensive materials and more sophisticated manufacturing technologies to enable 10 Gbps transmission. Consequently, achieving a 10 Gbps serial transmission over a backplane incurs a higher cost in terms of die area and power consumption.

The preceding example clearly shows that transceivers running at or below 3.2 Gbps are at a sweet spot; they are more cost-effective and power-efficient than both parallel interfaces and ultra-high-speed transceivers (running at 6 Gbps and 10 Gbps) for a large

majority of interconnect applications. This phenomenon has led to two diverging trends in the transceiver market:

1. Bandwidth-hungry applications (such as a backplane interconnect for terabit routers) have needs for 6 Gbps and 10 Gbps transceivers. These applications continue to push the performance envelope while trading off cost and power.
2. High-volume applications are well served by transceivers running at or below 3.2 Gbps.

**The Virtex-5 RocketIO GTP Transceiver**

Xilinx clearly recognizes the different requirements of the high-performance market segment, noting that the high-volume market segments have in some cases conflicting requirements. The vast majority of serial protocols run at or below 3.2 Gbps; examples include PCI Express Generation 1, Gigabit Ethernet, XAUI, SATA I and II, Serial RapidIO, CPRI, OBSI, and HD-SDI. Many emerging protocols such as JEDEC’s data converter interface and VESA’s DisplayPort also run at these relatively slow data rates. In reality, these established and emerging protocols represent more than 90% of current transceiver applications. Therefore, transceivers running at or below 3.2 Gbps are “transceivers for the masses.”

Xilinx has taken a truly innovative step and developed two different transceivers for its Virtex™-5 FPGA family. The first transceiver, the Virtex-5 RocketIO™ GTP transceiver, is designed for high-volume applications and covers data rates from 100 Mbps to 3.2 Gbps. Targeting the majority of system designers, the GTP transceiver is versatile, easy to use, power-efficient, and cost-effective.

The GTP transceiver is versatile because it is designed to support not only 8B/10B-based protocols such as the PCI Express Wrapper but also scrambling-based protocols such as SONET. (Table 1 is a complete list of applications supported by GTP transceivers.) Consequently, the spectrum of applications that can be supported by the GTP transceiver is limitless. In addition,

validation and characterization of the GTP transceiver occurs in application-specific settings to ensure standards compliance. The combination of these design and characterization approaches ensures the universal appeal of the GTP transceiver.

The GTP transceiver is easy to use because it enjoys the support of the best

FPGA CAD tools. The Xilinx® Virtex-5 RocketIO GTP transceiver wizard offers an intuitive GUI interface that allows you to select the GTP, clocking option, FPGA fabric interface, protocol stack, and encoding/decoding mechanism. After you have completed your selections, the tool generates a GTP wrapper with the necessary features.

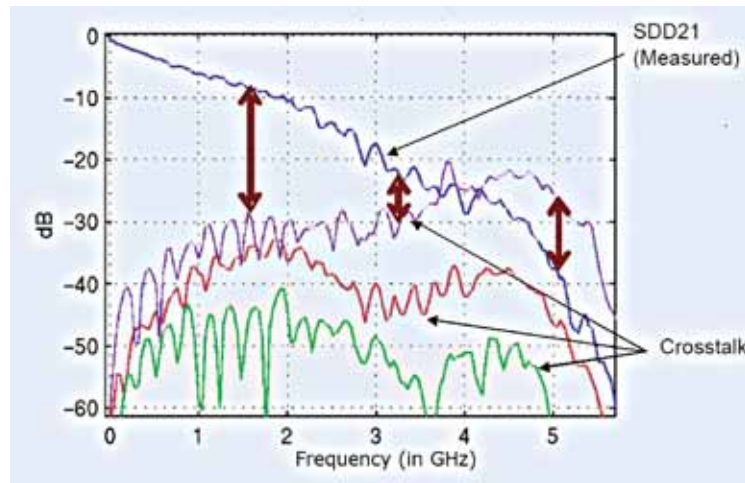


Figure 1 – Channel S-parameter and crosstalk



Figure 2 – ChipScope IBERT console

The Xilinx ChipScope™ Analyzer offers self-testing capabilities for the GTP transceiver by leveraging the integrated bit-error-rate tester (IBERT) feature built into the transceiver. The ChipScope IBERT console is shown in Figure 2.

Among the advanced features offered by the ChipScope Analyzer are channel performance measurement capabilities, automated eye scan capability for finding the best Tx and Rx settings, and transceiver and link status reporting. This comprehensive set of tool offerings greatly simplifies design and manufacturing efforts based on the GTP transceiver and is a key enabler for a large variety of applications.

As PCB boards become increasingly crowded, transceiver power consumption becomes a critical issue. Therefore, power efficiency was one of the top design objectives for the GTP transceiver. Average power consumption per GTP transceiver is substantially below 100 mW. In some cases, per-transceiver power consumption is as low as 60 mW. The universal appeal of low-power requirements further enhances the competitiveness of the GTP transceiver for power-sensitive applications.

As high-volume applications start to use embedded transceivers, cost has also become an important consideration. Consequently, Xilinx offers certain solutions in hard logic rather than in look-up tables (LUTs). For example, a hard-coded PCI Express protocol stack includes a physical layer based on the GTP transceiver, a link layer, and a transaction layer. This approach significantly lowers overall solution costs, and the increased cost-effectiveness makes GTP transceiver-based solutions even more attractive to high-volume/high-margin applications.

**Conclusion**

Transceivers at 3.2 Gbps or below are at a sweet spot; the vast majority of transceiver-based applications fall into this data-rate range. With its versatility, ease of use, power efficiency, and cost-effectiveness, the Virtex-5 GTP transceiver from Xilinx is ideally positioned in this market, a true multi-gigabit transceiver for the masses. 🌟

Market	Standard	Speed (Bits per Second)	Key Features
Telecom	OC-3/SDH STM-1	155 Mbps	• FIFOs can be Bypassed for Synchronous Operation
	OC-12/SDH STM-4	622 Mbps	
	OC-48/SDH STM-16	2.488 Gbps	
	OBSAI (Issue 1.0)	768 Mbps	
		1.536 Gbps 3.072 Gbps	
	CPRI (Version 2.0)	614 Mbps	
1.228 Gbps 2.457 Gbps			
SFI-5	2.448 - 3.125 Gbps	• Synchronous Clocking (Bypass FIFOs)	
Datacom	1G Ethernet (802.3z D5.0)	1.25 Gbps	
	XAU1 (802.3ae D5.0)	3.125 Gbps	• Loss of Signal (LOS)
	10G Base CX-4	3.125 Gbps (x4)	
Computing / Communication	PCI Express Specification (Rev 1.1)	2.5 Gbps	• Tx Receive Detect • Loss of Signal (LOS)/Idle state detect • Low Power States and OOB Beacon • Ground Referenced Termination
	Serial Rapid IO	3.125 Gbps	• Supports All Data Rates from 1.25-3.125G
	InfiniBand	2.5 Gbps	
Storage	Fibre Channel (Rev4.0)	1.0625 Gbps	• Rate Negotiation, Allows Tx and Rx to Operate at Different Speeds
		2.125 Gbps	
	SATA (Rev1.0a)	1.5 Gbps 3.0 Gbps	• Rate Negotiation for Gen1/Gen2 • LOS and Out-of-Band Signaling Beacon
SAS (Rev5)	1.5 Gbps 3.0 Gbps		
Video	SDI	143 Mbps 176 Mbps	• Internal AC Coupling Caps can be Bypassed for Video Standards • 2.97G is the New HD-SDI Standard in Development
	DVB-ASI	270 Mbps	

Table 1 – Applications supported by GTP