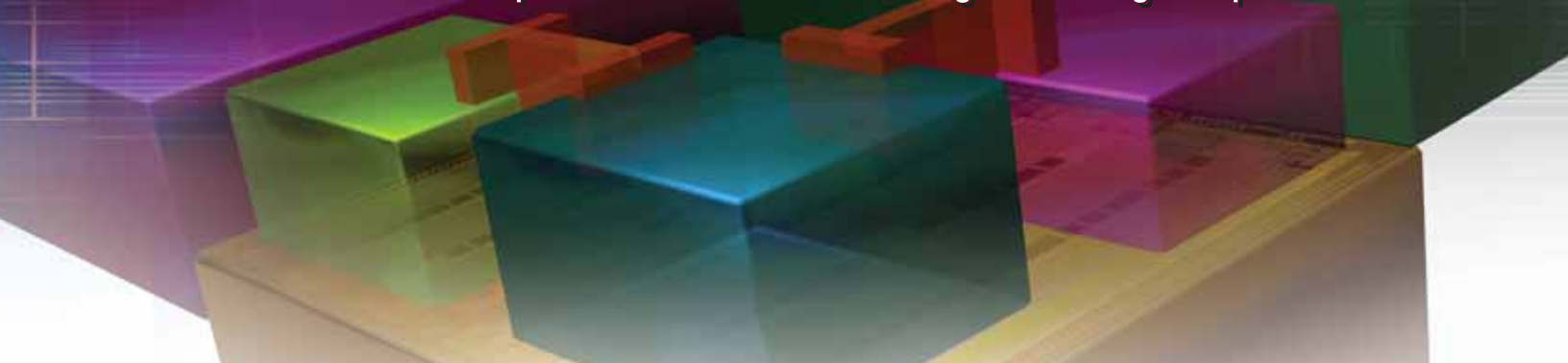
Introducing the Virtex-5 PCI Express Endpoint Block

With PCI Express quickly becoming the standard high-bandwidth interconnect, the Virtex-5 LXT PCIe Endpoint block enables a configurable single-chip solution.



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Currently dominating the desktop PC motherboard and graphics markets, the PCI Express (PCIe) interconnect is poised to supplant PCI and PCI-X as the dominant high-bandwidth interconnect for the server, enterprise, mobile, workstation, networking, communications, industrial control, and medical equipment markets.

With more than 58 form factors, including Express Card, Advanced TCA, Compact PCI Express, Com Express, and a cable spec, the PCIe protocol is becoming ubiquitous. The PCI Special Interest Group (PCI-SIG) maintains the PCIe specification (along with the PCI and PCI-X specifications) and holds compliance workshops.

The PCIe subsystem is a point-to-point interface that replaces and overcomes the limitations of bus-based PCI and PCI-X standards. PCIe Generation 1 (Gen1) offers 2.5 Gbps speed with low-voltage differential signaling (LVDS), embedded 8B/10B encoding, dual-simplex signaling, and message-based serial protocol.

With plans in place to increase bandwidth to 5 Gbps in Generation 2 and 10 Gbps in Generation 3, the PCIe bus is expected to be the dominant high-bandwidth interconnect for several years to come. (For more information on the PCIe specification or compliance information, visit *www.pcisig.com*.)

With scalable lane widths from x1 to x32 lanes and advanced features such as traffic classes, virtual channels, hot-plug, and power management, the Xilinx PCIe block provides support for a wide range of applications, from a simple upgrade from PCI to an x1 PCIe endpoint device to advanced high-bandwidth x8 PCIe communications endpoint devices.

Figure 1 shows the topology of a PCIe system. The CPU is connected to a root device and is responsible for configuring and enumerating all plug-and-play PCI Express endpoint devices in a system. Because the PCIe system is point-to-point, switch devices are necessary to grow the number of devices or endpoints in a system. A switch has one upward facing port and numerous downward facing ports. These downward facing ports connect to the working devices or endpoints of a system.

Although only one root exists in a system, there are one or more endpoint devices. For example, a standard PC motherboard provides three to seven expansion PCIe slots. With the integrated PCI Express Endpoint block, Xilinx® Virtex™-5 LXT FPGAs allow you to rapidly develop and deploy high value-added PCIe endpoint devices. The numerous value-added endpoint designs are the target applications for the FPGA-based configurable Virtex-5 LXT PCI Express Endpoint block.

The Virtex-5 LXT PCIe Endpoint Block

The Virtex-5 LXT PCIe Endpoint block (see Figure 2) implements the physical layer (PHY), data link layer (DLL), transaction layer (TL), and configuration layers of a PCIe endpoint device. The implementation of a small reset circuit and clock generation blocks require you to use the FPGA fabric.

The PCI Express Endpoint block capabilities include:

- Compliance with the PCI Express base specification, revision 1.1
- Choice of PCI Express Endpoint block or legacy PCI Express Endpoint block implementation
- x8, x4, x2, or x1 lane width
- Easy-to-use user interface similar to the familiar Xilinx LocalLink interface
- Integration of RocketIO™ GTP transceivers
- Spread-spectrum clocking support
- Low power operation
- Power management support
- Ability to use on-chip block RAMs for buffering
- Fully buffered transmit and receive
- Management interface to access PCIe configuration space and internal configuration
- Support for full range of maximum payload size (128 to 4,096 bytes)
- Capable of as many as two virtual channels (VCs)
- VC arbitration: round robin, weighted round robin, or strict priority
- 6 x 32-bit or 3 x 64-bit base-address registers (BARs) or a combination of 32-bit and 64-bit BARs
- BARs configurable for memory or I/O
- Memory BAR checking/filtering
- Non-memory transaction layer packet (TLP) ID checking/filtering
- Implements one PCI Express function
- Signals to the programmable fabric for statistics and monitoring
- Full documentation and reference example design

Virtex-5 GTP transceivers interface to the serial differential electrical signals of the PCIe specification. The PCIe block completes the physical logic that provides lane deskew. The DLL is responsible for data integrity and implements a user-configurable-sized retry buffer to retransmit packets that are received incorrectly without re-requests from the applications software. The TL provides Tx and Rx buffers and orders the packets to be transmitted. With capability for eight traffic classes and two virtual channels, great flexibility for packet arbitration is available.

High-Level Intregration

The Virtex-5 PCI Express Endpoint block allows you to implement a single endpoint device with one FPGA while leaving almost all of the FPGA programmable fabric avail-

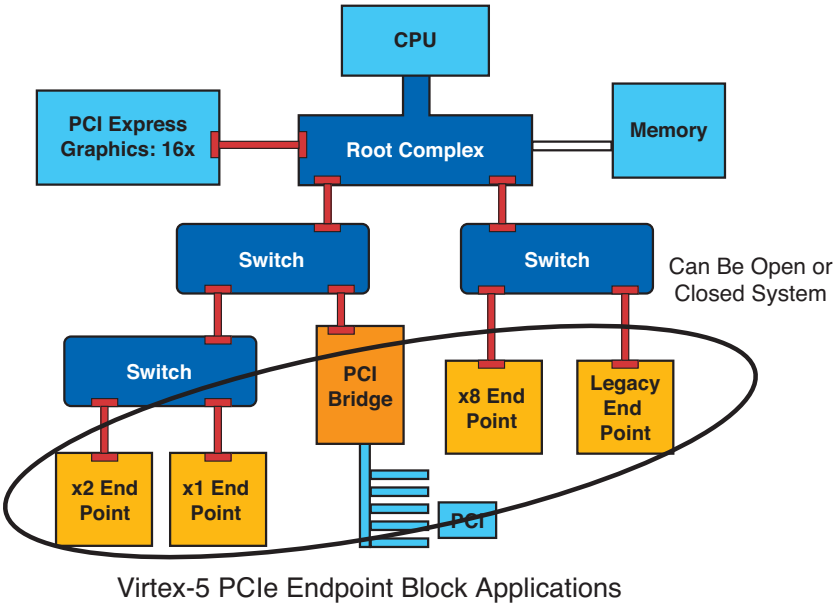

Figure 1 – PCI Express topology

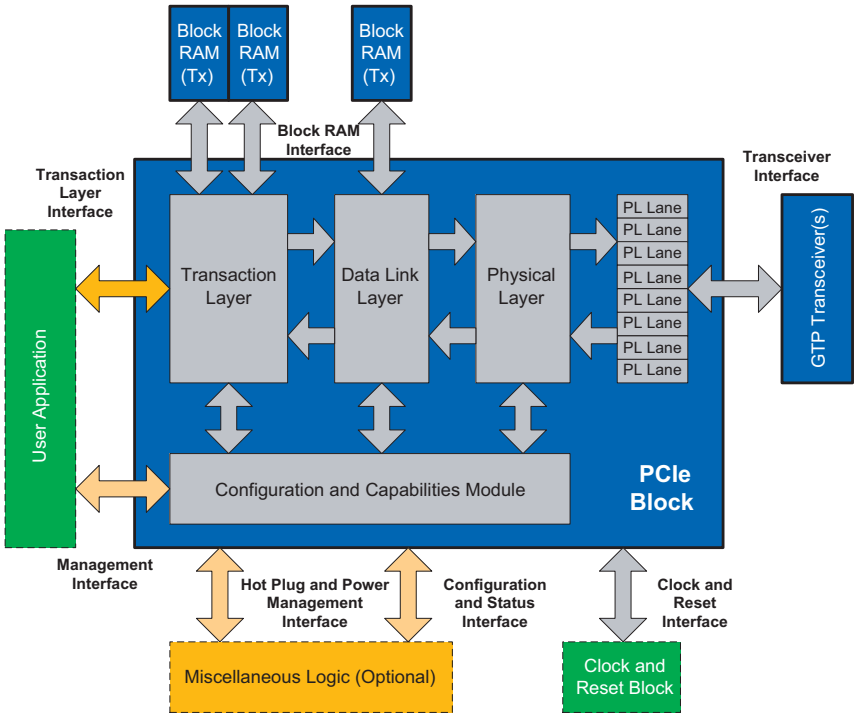

Figure 2 – Xilinx Virtex-5 LXT PCI Express Endpoint block

able for value-added endpoint application design functionality. The combination of the PCIe block, GTP transceivers, and the block RAM incorporate the majority of the logic required for a low-power, high-bandwidth, configurable PCIe endpoint port. The GTP transceivers support Gen1 2.5 Gbps serial rates while being electrically compliant to the PCIe specification. Some of the new transceiver features include power management support such as beacon and electrical idle detect and the spread-spectrum reference clock required in PC system motherboards.

The block RAM provides a scalable, user-configurable retry memory along with Tx and Rx FIFO for any packet size supporting one or two virtual channels. With complex configuration options of the PCIe block, GTP transceivers, and block RAMs, along with clock and reset logic, software automation provides quick and accurate configuration and interconnect of these functions.

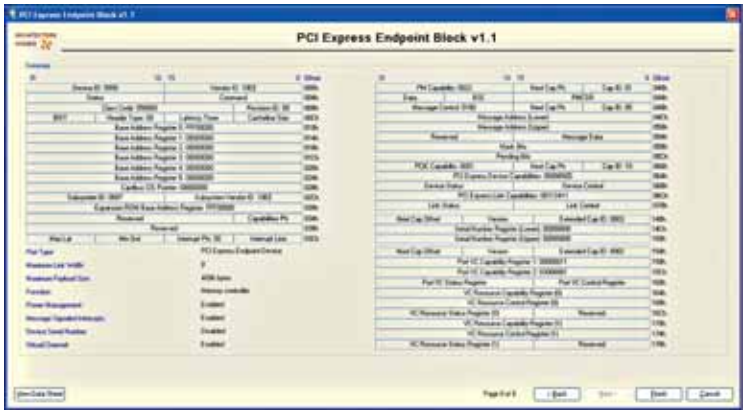

Figure 3 – Xilinx CORE Generator GUI

Figure 4 – ML523, ML555, and ML505 Virtex-5 LXT PCIe hardware reference boards

Using the PCI Express Endpoint Block

The Xilinx PCIe LogiCORE™ solution delivers wrappers through the CORE Generator™ software GUI flow of the ISE™ tool, which makes it easy to use the PCIe block and still provides full flexibility of the configurable features and capabilities of the high-bandwidth PCI Endpoint block. The configuration capabilities of the PCIe block are abstracted into several self-checking and instant-feedback menus that walk you through the configuration of key design elements (Figure 3).

The LogiCORE wrappers connect the PCIe block with the GTP transceivers and block RAMs. They also create and connect the clock and reset logic blocks to the PCIe block. You can customize the clock and reset RTL blocks to address advanced system requirements. In addition to connecting the various hardware resources to the PCIe endpoint block, the advanced wrapper provides value-added features such as the user-friendly interface similar to Xilinx LocalLink, the memory BAR, and non-memory TLP ID checking and filtering.

Ready to Provide High Bandwidth

The launch of the Virtex-5 PCIe block in the Virtex-5 LXT device not only provides the block and PCIe wrapper support, but also includes extensive system design aids. Memory endpoint and programmed input/output (PIO) reference designs are included in the deliverables. These designs serve as a training aid, quickly bringing up a simple user application to test in hardware.

In addition, the successful PCI-SIG compliance achieved with this design greatly speeds up the path to compliance for the users of the PCIe block in Virtex-5 devices. Xilinx provides a suite of hardware reference boards such as the ML523 characterization board, ML505 embedded design reference board, and the ML555 x8 high-data-bandwidth PCIe board to enable you to build and test PCIe systems (Figure 4).

Compliance testing requires a complete design with a demonstrable function, hardware board, software device driver, and application software to demonstrate interoperability with PC motherboard systems. The memory endpoint and PIO reference designs provide all of the above. Sample device drivers for Windows XP, Windows Server 2003, Windows Vista, or Linux are available by request. As the reference design function emulates a memory aperture, a simple test is provided to demonstrate the design operation.

This Virtex-5 LXT device and Xilinx reference hardware boards are listed on the PCI-SIG integrators list. For PCI-SIG-complaint Xilinx solutions, visit *www.pcisig.com/developers/compliance_program/integrators_list/pcie.*

Conclusion

The Virtex-5 LXT PCI Express Endpoint block, combined with the GTP transceivers and block RAMs, provide an extremely high level of integration for you to efficiently and quickly build high-performance, fully compliant PCIe systems in a single device. Xilinx developed and delivered the Virtex-5 PCI Express solution with a focus on end-user requirements for ease of use, legacy design migration, powerful yet flexible features and capabilities, system-level compliance, and cost.

For more information, visit *www.xilinx.com/virtex5.*