

# PCI Express Markets, Trends, and Applications

The Virtex-5 LXT device's built-in PCI Express solution enables significant power and area savings.

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End users are adopting multimedia-enabled devices rapidly; you need look no further than iPod video or YouTube-like blog sites. As users consume this type of rich data, the need for efficient storage and higher connectivity speeds becomes critical.

Today, the megahertz debate has been replaced with the gigabit-per-second debate, as the focus shifts from processing speed to high-speed interconnect. A host of serial standards have come into play. The key market requirements governing these standards are:

- Scalable performance
- An extensible feature set to adapt to various use models (chip-to-chip, backplanes, cable)
- Interconnects suitable for multiple market segments and applications
- Implementation of cost-effective solutions in mainstream high-volume technology

One of the key serial standards to emerge is PCI Express (PCIe), a third-generation I/O interconnect introduced in 2002 to provide a scalable path from PCI and PCI-X (see Table 1). PCIe has become the standard interconnect of the PC industry and is rapidly gaining momentum in other applications as well (Figure 1). It promises scalability, an extensible feature set, multiple market suitability, and cost-effectiveness.

Key highlights of PCIe include:

- A high-speed serial standard offering bidirectional communication at 2.5 Gbps line rates per lane
- Layered packet-based architecture, enabling modular design
- Bandwidth enhancement (as much as 80 GB) through easier scalability – 1, 2, 4, 8, 16, and 32 lanes
- Advanced features like reliability, power management, and hot plug
- Support for next-generation three-dimensional/multimedia traffic through virtual channels, traffic classes, and quality of service (QoS)
- Ease of use through new form factors and innovative designs, enabling applications targeted to multiple market segments
- Software preservation by supporting legacy PCI architecture and infrastructure

Tremendous acceptance, design wins, and strong customer feedback have propelled our understanding of the inherent benefits of PCI Express in our customers' applications. To create solutions for solving tomorrow's problems today and keep pace with rapidly changing times, Xilinx has introduced a hard PCI Express Endpoint block in its Virtex™-5 LXT devices (Figure 2).

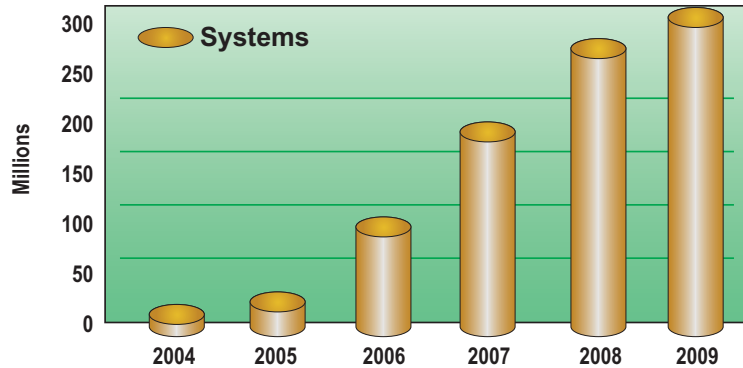
The salient features of the PCIe Endpoint block are:

- Full-featured and compliant to PCIe base specification v1.1
  - Highly configurable PCIe endpoint solution
- Passed compliance/interoperability tests at PCI plug-fest ([www.pcisig.com/developers/compliance\\_program/integrators\\_list/pcie](http://www.pcisig.com/developers/compliance_program/integrators_list/pcie))
- Supports 1-, 2-, 4-, or 8-lane implementations
- Meets all key requirements
  - Electrical signaling
  - Protocol (CRC, automatic retry)
  - QoS
  - Hot-pluggable

PCI Specification	Bus Width	Transfer Rate	Lane Width	Line Rate	Max Data Bandwidth
PCI 1.0	32 bits	33 MHz			133 Mbps (half-duplex)
PCI 2.x	64 bits	33-66 MHz			266-533 Mbps (half-duplex)
PCI-X 1.x	64 bits	133 MHz			Up to 1 Gbps (half-duplex)
PCI-X 2.0	64 bits	266-533 MHz			Up to 4 Gbps (half-duplex)
PCI Express 1.x			1 lane	2.5 GHz	Up to 500 Mbps
			2 lane	2.5 GHz	Up to 1 Gbps
			4 lane	2.5 GHz	Up to 2 Gbps
			8 lane	2.5 GHz	Up to 4 Gbps
			16 lane	2.5 GHz	Up to 8 Gbps
			32 lane	2.5 GHz	Up to 16 Gbps
PCI Express 2.0*			1-32 lanes	5 GHz	Up to 32 Gbps

\* The PCI Express 2.0 specification is "still under construction."

Table 1 – PCI/PCI-X/PCIe specification and bandwidths



Systems = PCs + Servers + Workstations + Embedded Systems

Figure 1 – PCI Express momentum

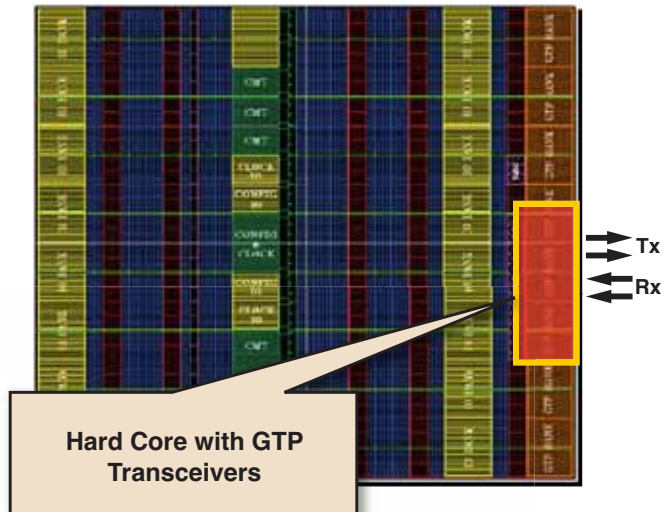
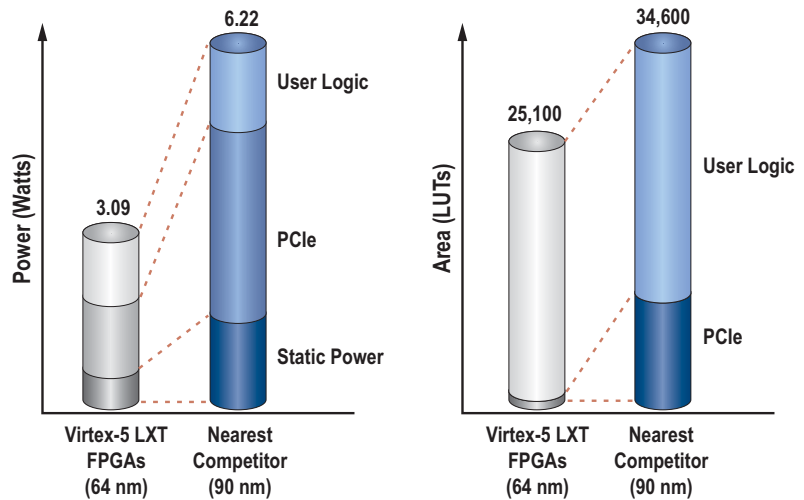


Figure 2 – PCIe Endpoint block in the Virtex-5 LXT FPGA

- Uses Xilinx® RocketIO™ GTP transceiver blocks
  - PCI Express electrical support
  - 100-MHz direct reference clock
- Saves resources
  - Integrated in all Virtex-5 LXT devices
  - Adjacent to GTP transceivers
- Ease of design
  - Shortens design cycles
  - Simplified, intuitive design flow
- Low cost and low power
- Packet buffering with configurable block RAM
  - Rx buffer
  - Tx buffer
  - Retry buffer
- Simple transaction layer interface for easy integration
- Signals available to fabric for statistics and monitoring
  - credit status, max payload size, error signals
- As many as two virtual channels for QoS
  - Round robin, weighted round robin, or strict priority

Power Consumption and Area Required to Implement a Typical Design Including 8-Lane PCIe Endpoint



XC5VLX30T versus 2SGX60D. Target Frequency = 200 MHz. Worst-case process 25K LUTs, 17K flip-flops, 1 Mb on-chip RAM, 64 DSP blocks, and 128 2.5V I/Os. Based on Xilinx tool v8.2 and competitor tool v6.01.

Figure 3 – Power and area savings of a high-performance Virtex-5 LXT PCIe solution

the Intel Developers Forum in September 2006. Xilinx also endorses this initiative, which extends the PCIe architecture to enable emerging application accelerators.

- Low power and reduced area. Applications that need higher performance but are designed to smaller form factors can use the Virtex-5 LXT solution (Figure 3). The PCIe Endpoint block allows you to be able to choose a smaller device and still achieve significant power and cost savings.

- Bridging legacy and disparate standards to PCIe. The movement of legacy applications to new form factors optimized for PCI Express requires bridging functions between legacy standards and PCI Express. The new Virtex-5 LXT platform offers the customization and logic resources to enable this transition as well as bridging to other serial standards.

- Scalable solution. The PCI Express protocol is here to stay, but the protocol itself and use models are in rapidly

### Designing with the Virtex-5 LXT PCIe Block

PCI Express has gained considerable momentum, with broad acceptance in the PC industry. Engineers designing with Virtex-5 LXT FPGA-based PCIe endpoints can also lead the proliferation of PCI Express in new markets by leveraging these advantages:

- Faster time to market. Existing ASSPs do not support PCIe today; FPGAs enable bridging between proprietary parallel interfaces and PCIe. In addition, evolving add-ons to the PCI Express standard discourage ASIC/ASSP starts until a broad market base has been created. A case in point is the recent “Geneseo” architecture announcement by Intel and IBM at

### Xilinx PCI History

Xilinx has been at the forefront of the PCI/PCI-X/PCIe technology. Significant achievements include:

- 1996 – Industry’s first PCI core for FPGAs
- 1999 – Industry’s first 64-bit, 66-MHz PCI solution
- 2000 – Industry’s first 64-bit, 133-MHz PCI-X solution
- 2003 – Industry’s first PCIe solution
- 2005 – Industry’s first PCIe PIPE solution – Xilinx + NXP Semiconductors
- 2006 – Industry’s first FPGA Express Card solution – Xilinx + NXP Semiconductors
- 2006 – Industry’s first FPGA with built-in PCI Express Endpoint block

evolving phases. Designing with Virtex-5 LXT PCIe Endpoint blocks enables you to scale from 1- to 4- to 8-lane link-widths in the same Virtex-5 family. This allows you to future-proof the system and the equipment. In addition, because PCIe is inherently compatible with legacy PCI and PCI-X architectures, scaling and designing Virtex-5 LXT FPGA-based PCIe solutions will preserve software investments and extend infrastructure life.

- Form factors supported. Virtex-5 LXT RocketIO GTP transceivers offer significant power advantages over competing FPGA/ASSP solutions. This enables designers to consider Virtex-5 FPGAs in new markets. You can use the inherent advantages of the 65-nm FPGA to support multiple form factors by using scalable logic density for different solutions. For example, a desktop solution in an add-in card form factor can be scaled to a lower power Express Card form factor using similar/identical FPGA resources. Conversely, a desktop add-in card form factor PCIe solution in a Virtex-5 LXT FPGA can be easily scaled up to support the transition to high-performance form factor solutions like ATCA, uTCA, and server I/O module.

Applications	Form Factors	Link Width (Typical)	Data Bandwidth	Prominent Feature Required
Enterprise	HBAs, Server I/O Module	x1	250 Mbps	High Reliability Scalability Error Recovery Reduced Board Space Reduced Power Budgets
		x4	1 Gbps	
		x8	2 Gbps	
Desktop	Add-In Card	x1	250 Mbps	Legacy Support to Existing (PCI) Software Reduced Board Space Reduced Power Budgets Ecosystem Existence High Availability
		x4	1 Gbps	
		x8	2 Gbps	
		x16	4 Gbps	
Mobile	Express Card, Mini-Card	x1	250 Mbps	Reduced Power Budgets High Reliability Power Management Capability
Communications	HBAs, ATCA, Server I/O Module	x4	1 Gbps	High Availability High Performance Interoperability Reliability
		x8	2 Gbps	
Embedded Platforms	Integrated Endpoints, Custom Cards, Mini-Card	x1	250 Mbps	Low Cost Reliability High Availability Ease of Use and Integration

Table 2 – Virtex-5 LXT PCIe Endpoint applications

### PCI ExpressFabric Topology

The PCI ExpressFabric™ topology, referred to as a hierarchy, comprises a root complex (RC), multiple endpoints (I/O devices), a switch, and a PCI Express/PCI bridge, all interconnected through PCI Express links.

An RC denotes the root of an I/O hierarchy that connects the CPU/memory subsystem to the I/O. A root complex may support one or more PCI Express ports, for example, Intel chipset(s).

A switch is defined as a logical assembly of multiple virtual PCI-to-PCI bridge devices, which forward transactions using PCI bridge mechanisms, namely address-based routing such as the IDT PCI Express switch.

Endpoint refers to a type of device that can be the requester or completer of a PCI Express transaction, either on its own behalf or on behalf of a distinct non-PCI Express device, for example, a PCI Express-attached graphics controller.

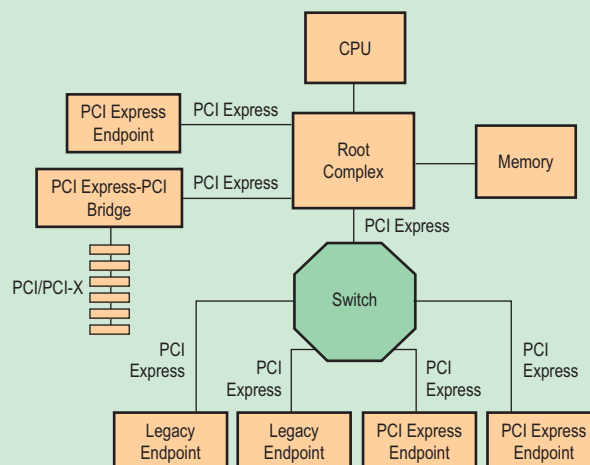


Figure 4 – PCI Express topology

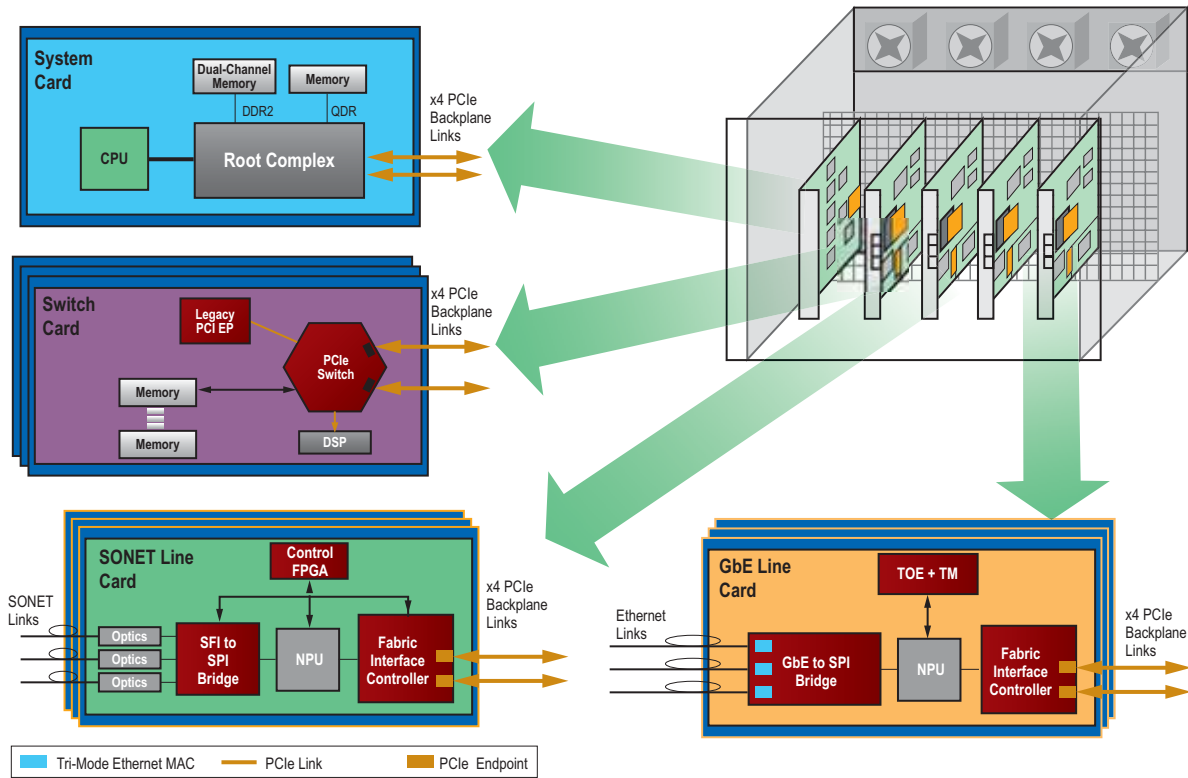


Figure 5 – PCIe in a communication system

Virtex-5 LXT FPGAs with built-in PCIe Endpoint blocks can easily be designed in all form factor applications, as shown in Table 2.

Figures 5 and 6 outline applications using Virtex-5 LXT PCIe Endpoint block capabilities to aggregate multiple-source traffic and bridge protocols to PCI Express.

**Conclusion**

The Virtex-5 LXT platform, with built-in PCIe Endpoint blocks and RocketIO GTP transceivers, offers great value by providing a full-featured, fully compliant PCIe solution. Say goodbye to IP licensing and hello to lower power and fewer utilized logic resources. You can achieve significant cost savings by targeting smaller FPGA devices with 50% of the power of soft-IP alternatives. Built-in hard blocks deliver guaranteed functionality and ease of use by reducing design time.

Thus, the Virtex-5 LXT platform offers unique built-in PCIe capabilities in a fast, low-power, 65-nm FPGA, launching a new era of efficient PCIe system development.

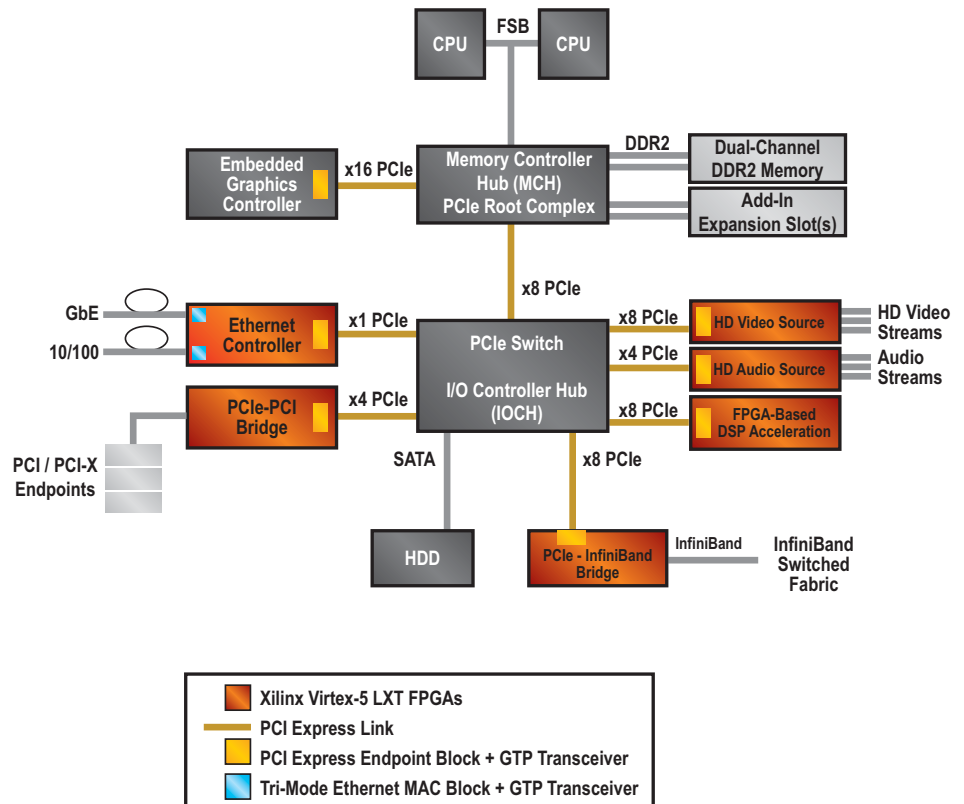


Figure 6 – PCIe in a high-end desktop/server system