

# Asynchronous Sample-Rate Conversion Between AES Audio Streams

Xilinx Virtex-5 FPGAs provide the perfect platform for implementing AES digital audio sample-rate conversion.

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The diversified uses and ever-changing innovations for digital video and audio continue to drive the fast-paced proliferation of equipment for audio, video, and broadcast (AVB). Today's AVB equipment demands better image quality, higher resolutions, higher bandwidths, more audio/video channels, and the combining of previously separate but related functions such as HD-SDI, audio multiplex, audio demultiplex, and asynchronous sample-rate conversion (ASRC).

Xilinx® FPGAs have kept pace with customer integration needs by incorporating silicon features, facilitating the absorption of less integrated, complex, and expensive ASSP chips. One such ASSP chip function, ASRC, can be integrated into Xilinx FPGAs by leveraging diffused silicon features known as DSP48E slices and block RAMs to build sophisticated filter functions.

Free Xilinx application notes and reference designs have also kept pace with our customers' need to integrate sophisticated algorithms. The ASRC reference design correctly handles synchronous sample-rate conversion and the far more complex ASRC called for in most audio/video applications.

Simpler "synchronous-only" methods, offered by many ASSP chips and FPGA IP suppliers, can be smaller in terms of utilization per audio channel; however, when applied incorrectly to asynchronous applications, these methods have one or both of the following artifacts:

- The input-to-output latency changes because of accumulating delay
- Artifacts are produced in the audio, such as skipping samples or repeating samples

Both of these cases represent undesirable distortions.

**Understanding Sample-Rate Conversion**

Before diving into the theory of digital sample-rate conversion, you should look at the basic types of problems audio/video engineers are trying to solve. A few applications exist where you could use a fixed-rate synchronous conversion, such as a 48-KHz input converted to a 44.1-KHz output using the same clock source, or an output clock derived from the input clock. However, more likely is the asynchronous case, where input and output clocks are completely independent, such as two boards communicating audio between them. The different clock oscillators can be the same nominal frequency but several parts-per-million different.

The Xilinx ASRC reference design for the asynchronous case of independent input and output clocks provides two important and difficult design functions:



Figure 1 – ML571 board and frame synchronization demonstration board with an ASRC to match the output digital audio rate to the output digital video rate.

- Automatically and accurately monitoring the input-to-output ratio and sample-rate changes
- Adapting the filter function (filter coefficients) on the fly to provide the highest performance

Supporting ASRC for digital audio with an FPGA means that you can now significantly save costs for every SDI interface in your system – and in many systems, there are many channels.

The Xilinx ASRC IP is very high performance, with a worst-case input-to-output signal-to-noise ratio of -125 dB. It also supports conversion for multiple audio-input frequencies to multiple audio-output frequencies. The rate conversion algorithm

adjusts on the fly, maintaining high performance with no special attention needed for input and output clocks. You can verify all of this with the IP running the Xilinx ML571 Serial Digital Video demonstration board shown in Figure 1.

Best of all, the broad functionality and high-performance ASRC IP is free.

**Sample-Rate Conversion Theory**

Figure 2 illustrates conceptually the general case of up or down conversion. The conversion ratio can vary continuously by rational numbers with fractional values. The diagram shows the up conversion process (creating many more samples and time positions to choose from) followed by down conversion (judiciously choos-

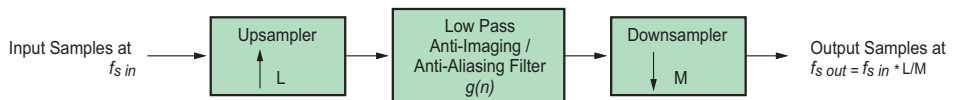


Figure 2 – Classic conceptual data path for sample-rate conversion

## The ASRC adjusts the de-embedded audio to match the output video stream clock rate, where it can then be re-embedded into the output SDI video stream.

ing the samples in the output datastream that most closely match the positions of the desired samples). The anti-imaging/anti-aliasing filter in the center of the data path ensures that the spectral content is less than half the Nyquist rate of both the input and output sampling frequencies.

Figures 3 and 4 show that for every output sample location or output phase, a different set of sub-filter coefficients is required

because the inputs are in different locations relative to that output phase. The sub-filter, having a set of coefficients that align with the input sample positions, is formed by interpolating the prototype filter coefficients. When this sub-filter is convolved with the corresponding input samples, the output sample of interest is produced. This process repeats, with new sub-filter coefficients interpolated for each output sample.

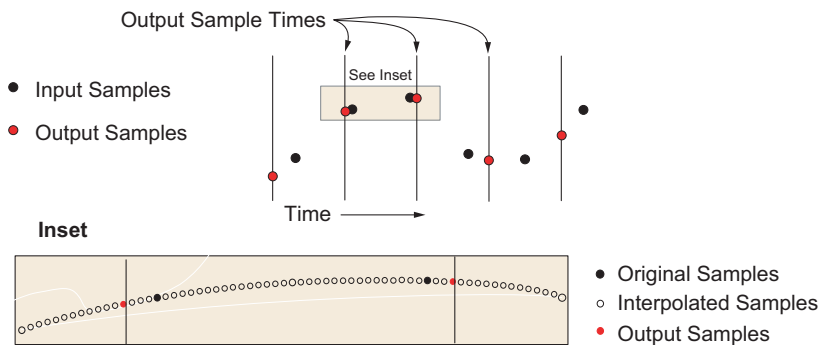


Figure 3 – Output sample position relative to the original sample position dictates which interpolated samples to use.

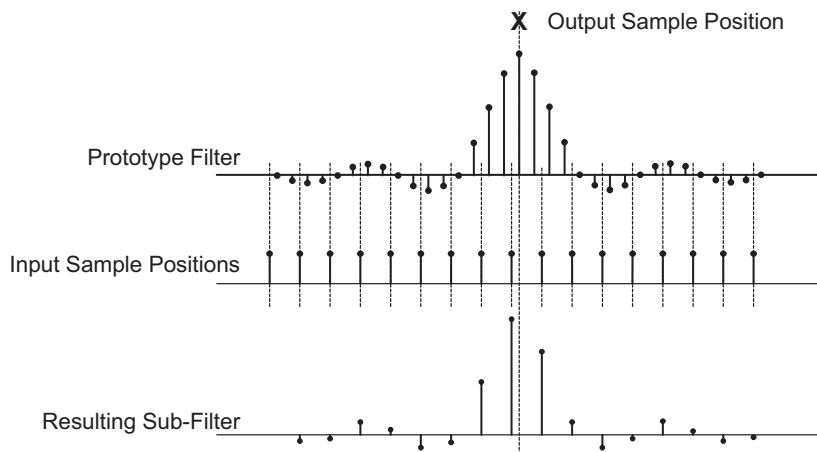


Figure 4 – Prototype filter centered at output sample position

### ASRC Example Implemented on the ML571

The simple function known as frame synchronization of video provides a great demonstration of where you might use ASRC. Video can be stored in a frame buffer at some rate and removed at a fractionally different rate. This process can be useful if two pieces of video equipment are not “genlocked” together and operate at different pixel rates.

The result is the occasional need to add or drop a frame of video data. Your eye probably would not notice an added or dropped frame of video on your TV screen, but the human ear is very good at detecting discrepancies in added or dropped audio. The solution is to remove the audio from the starting video stream and reinsert it in the resulting video stream at a fractionally different rate, matching the output audio rate to the new output video rate. The Xilinx ASRC reference design is perfect for this task.

As an example, let’s connect two boards with SDI video running at slightly different frequencies because of the different clock oscillators on each board. The receiving board demultiplexes the embedded AES digital audio from the video stream and sends it to the ASRC. The difference in clock frequency between the two boards causes the frame buffer synchronization logic to add or drop video frames. The ASRC adjusts the de-embedded audio to match the output video stream clock rate, where it can then be re-embedded into the output SDI video stream. The difference in clock frequencies between the two boards causes the frame buffer synchronization logic to add or drop video frames. The ASRC adjusts the de-embedded audio to match the output video stream clock rate, where it can then be re-embedded into the output SDI video stream.

For more information about frame buffer synchronization and asynchronous sample-rate conversion techniques, see XAPP514, “Audio/Video Connectivity Solutions for the Broadcast Industry,” at [www.xilinx.com/bvdocs/appnotes/xapp514.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp514.pdf).

**Block Diagram and Specification Highlights**

The simple diagram in Figure 5 illustrates two key design elements required in ASRC. The first element is determining the changes between input sample rate and required output sample rate, labeled “ratio control.” The second element within the “re-sampler” is a set of prototype filters that are modified depending on the statistics reported by the ratio control.

The ASRC reference design converts stereo audio from one sample frequency to another. The input and output sample frequencies can be an arbitrary fraction of one another or the same frequency, but based on different clocks. The output is a band-limited version of the input re-sampled to match the output sample timing. The reference design has the following features:

- Fully asynchronous operation
- Expandable to multiple channels
- A -125 dB THD+N worst case with -130 dB THD+N typical
- A 24-bit audio word width in and out, with 31-bit internal math precision and round away from zero
- Automatic input-to-output sample ratio monitoring with continuous filter modification

- Continuous rational/fractional ratio, up conversion, 8:1
- Continuous rational/fractional ratio, down conversion, 1:7.5
- Continuous input-to-output rate monitoring with adaptive filtering
- Input/output rates 8 KHz-192 KHz, continuous
- Low deterministic latency

The reference design has an interpolated coefficient FIR filter coded with Virtex™-5 DSP48E slices as the primary math element and block RAM for input sample buffers and prototype storage.

**Conclusion**

The need to maintain different input-to-output audio rates for varying numbers of digital audio channels and support new AVB functions is a tremendous challenge. Throw in varying protocols, memory management, different sized payloads, and a variety of different system interfaces, and it is easy to see how these designs require high-performance, cost-effective flexibility that ASSPs and ASICs cannot offer. These challenges open up opportunities for Virtex-5 devices because these devices can enable equipment vendors to provide solutions to the ever-evolving AVB equipment landscape. 🌈

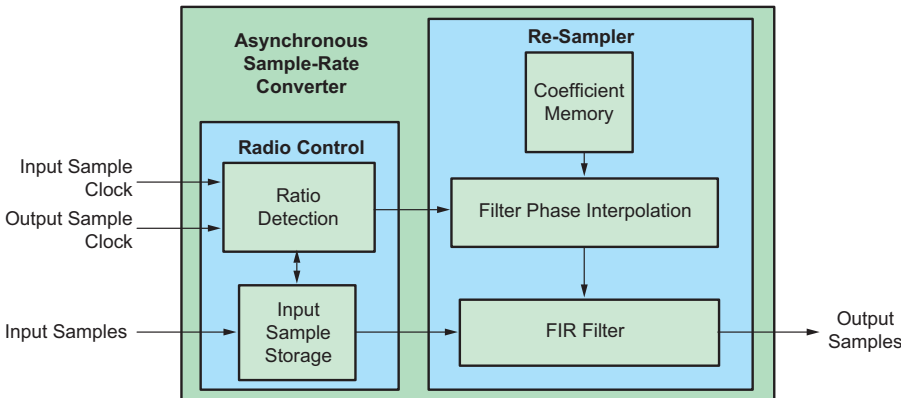


Figure 5 – Xilinx ASRC reference design top-level block diagram



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