

Enhancing System Management and Diagnostics with the Virtex-5 System Monitor

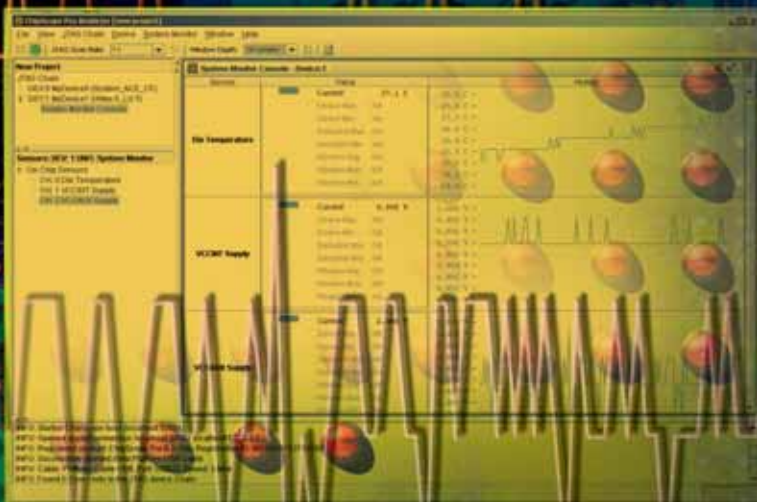
You can use the Virtex-5 System Monitor to greatly increase environmental monitoring coverage of your FPGA design.

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The telecommunications industry demands high availability; when you pick up the telephone, you expect to hear a dial tone. As broadband providers start to compete for voice and video (with the deployment of so-called “triple-play” services), customers expect the same high availability.

High availability is only possible by building redundancy into the hardware that makes up the system. However, to effectively manage this redundancy, the system must be able to monitor its own operating conditions and switch to backup hardware in the event of a failure before the customer notices any downtime. Close monitoring of the physical environment allows for preemptive action in the event of a failing component. This involves monitoring the physical environment inside the chassis, using various sensors to record such variables as temperature, supply voltages, humidity, and cooling performance.

FPGAs are important building blocks in high-availability infrastructure. Therefore, the on-chip environment of the FPGA and its immediate surroundings within the system should be carefully monitored. The Xilinx® Virtex™-5 System Monitor facilitates easier monitoring of the FPGA and its external environment.



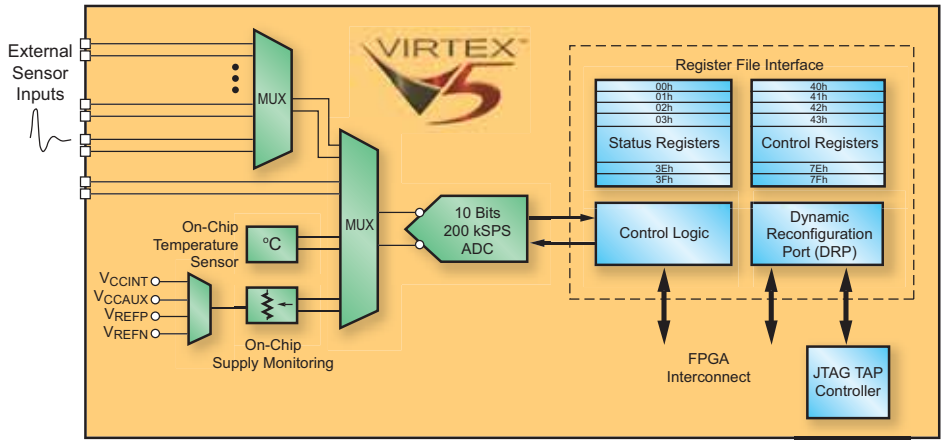


Figure 1 – Virtex-5 System Monitor

Virtex-5 System Monitor

The Virtex-5 System Monitor allows you to easily access information about the FPGA on-chip (die) temperature and power supply conditions. The system monitor also provides access to external sensor information through external analog input channels (monitoring as many as 17 external sensors). Access to this information involves little or no design effort, depending on the required functionality. Common functionality like alarms, automatic channel sequencer, and data averaging are available within the System Monitor block, enabling you to develop a solution easily.

Figure 1 shows a block diagram of the Virtex-5 System Monitor. The system monitor is built around a 10-bit, 200 kilosample-per-second analog-to-digital converter (ADC). The analog input range of the ADC is 0V-1V. At a resolution of 10 bits, the ADC can resolve an input voltage to an accuracy of approximately 1 mV.

As shown in Figure 1, both the on-chip sensors and external analog input channels are connected to the ADC input using analog multiplexers. Therefore, the output voltages from various sensors must be sequentially converted to a digital word by the ADC. These measurement results are written to status registers, where they are easily read using the FPGA fabric, or externally through the FPGA and PC board JTAG infrastructure. The System Monitor control registers can be written or read

using the same interfaces. The control registers configure the System Monitor operation (for example, selecting sensor channels for measurement, program alarm limits, and sensor averaging). The System Monitor is fully functional shortly after power-up and does not require the FPGA to be configured for correct operation. By default, only the on-chip sensors are monitored after power-up; however, you can also enable external analog inputs. Measurement information can only be accessed through the JTAG test access port (TAP) before configuration.

User Alarms

One of the useful built-in features of the System Monitor is its ability to generate alarm signals for the on-chip sensors. As a designer, you can specify the threshold limits for these alarm signals. The System Monitor can autonomously monitor the sensors and alert the system only when an alarm condition is detected.

The System Monitor also contains a factory-set alarm condition called over temperature (OT). If you enable this feature, the System Monitor can request a full chip power-down if a die temperature greater than 125° C is detected. Chip power-up is initiated after the die has cooled to a level that you specify. The System Monitor continues to operate and monitor the on-chip sensors during chip power-down.

The OT functionality is disabled by default and must be explicitly enabled.

Checking the Checker

Using the Virtex-5 System Monitor to provide accurate and reliable environmental information requires reliability checks on the measurement data and system monitor operation. The System Monitor has a number of features that help to confirm reliable operation. Built-in auto-calibration of the ADC and sensors correct any drift in the analog measurement system because of the operating environment. Self-check features also allow the system host to monitor the operation of the System Monitor.

Leveraging System Monitor JTAG Access

A novel feature of the Virtex-5 System Monitor is the ability to access the full functionality of the block using the JTAG TAP. By enabling analog testing and access to analog information, you can obtain greater value and efficiencies using the existing JTAG infrastructure in the system. This access is available before configuration of the FPGA for use as part of a PC board test scheme in production, or during normal operation to facilitate a debugging effort.

To facilitate off-chip measurements such as supply voltages and currents on the PC board, you can use special JTAG commands to enable external analog inputs before FPGA configuration. Even after FPGA configuration, the System Monitor does not require an explicit instantiation in your design, thereby allowing full access to its features for debugging work through the JTAG TAP, even at a late stage in the design process. To ensure the availability of the System Monitor, the only requirement is that the correct PC board support must be in place. This involves the connection of an external 2.5V reference IC as described in the System Monitor User Guide (www.xilinx.com/bvdocs/userguides/ug192.pdf).

Figure 2 illustrates a typical diagnostic application where the physical operating environment of the FPGA is monitored during normal operation. In the example illustrated in Figure 2, the System Monitor is used to look at the voltage (IR) drop in the power distribution system (PDS) during a period of heavy current demand starting at time t0. The temperature of the FPGA is also monitored during this period

of high activity. Potential issues with the power supply or PC board design can be quickly identified during development. The JTAG access also provides an easy way to confirm that adequate cooling is in place for a particular design. The ChipScope™ Pro Analyzer provides an easy way to access the System Monitor; however, access can easily be incorporated into other JTAG test and programming environments.

System Integration

In addition to convenient access through the JTAG TAP, full access to the System Monitor control and status registers is also provided through the FPGA fabric. These registers can be configured and read at any time from the fabric. Dual access to the System Monitor registers by the JTAG TAP controller and fabric interface is permitted, and an

arbitration scheme is available to manage possible contention.

You can also define the contents of these registers when the System Monitor is instantiated in a design and initialized during FPGA configuration. Thus, the System Monitor can be configured to start up in a user-defined mode of operation post-configuration. The fabric interface is known as the dynamic reconfiguration port (DRP). The DRP is a parallel 16-bit synchronous data port (similar to block RAM).

For more advanced applications where greater control over the System Monitor is required, the DRP allows the System Monitor to be easily mapped into the peripheral address space of a hard or soft microprocessor. Figure 3 illustrates a typical system management application where the MicroBlaze™ processor is running a protocol-like intelligent platform management interface (IPMI) and communicating with the system host over management channels like Ethernet or even a simple UART/modem.

The System Monitor also provides an important microprocessor peripheral in the form of a general-purpose ADC. This is the first time analog peripherals like those commonly found in microcontrollers have been integrated into an FPGA. Full control over the ADC operation is supported. The ADC offers a number of sampling modes and can support unipolar, bipolar, and full-differential analog input schemes.

Conclusion

The Virtex-5 System Monitor delivers a greatly simplified solution for common on-chip and external environmental monitoring needs. Minimal development and design effort are required to access the functionality. By interfacing the System Monitor to the JTAG TAP controller, JTAG functionality has been extended into new application areas, thus enabling new test capabilities.

We would like to hear your comments and feedback regarding any topics touched on in this short article; in particular, how our development team can better support your system monitoring and test requirements.

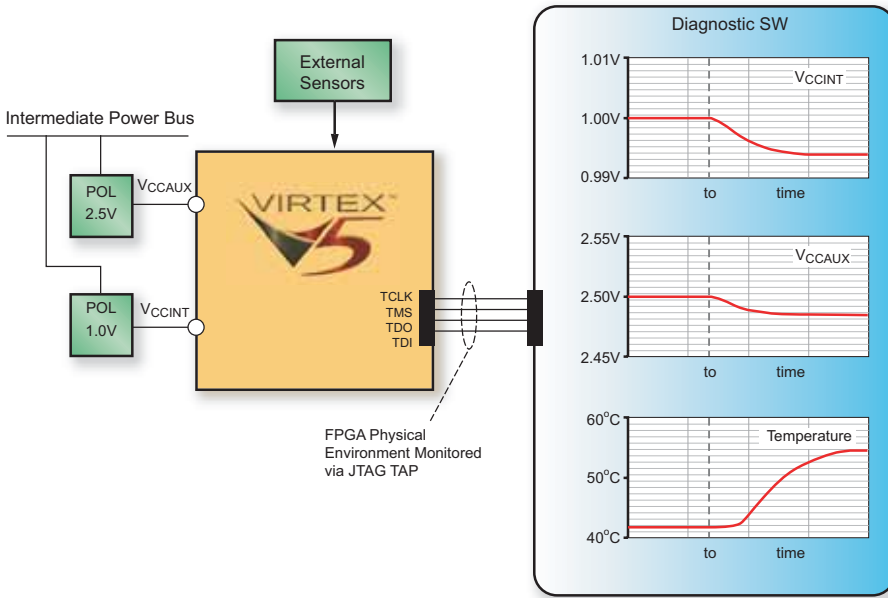


Figure 2 – You can access System Monitor measurements through the JTAG TAP.

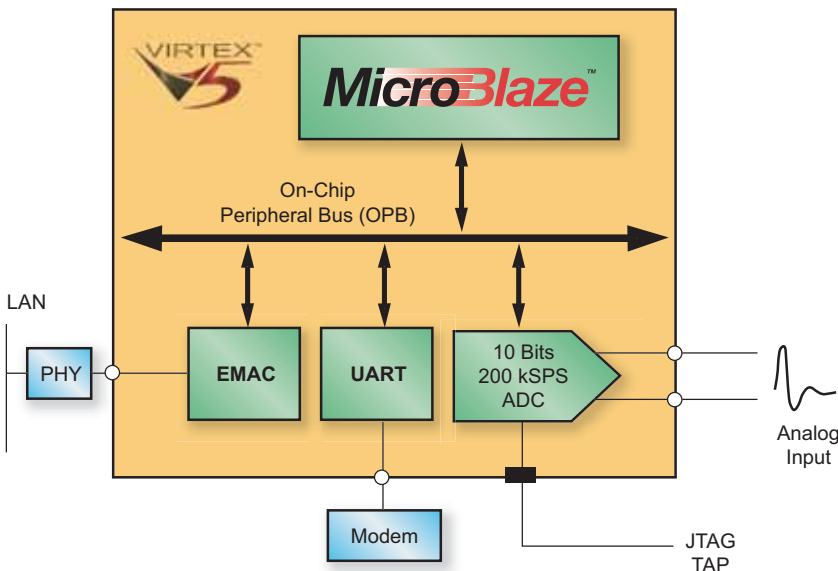


Figure 3 – System Monitor (or ADC) as a microprocessor peripheral