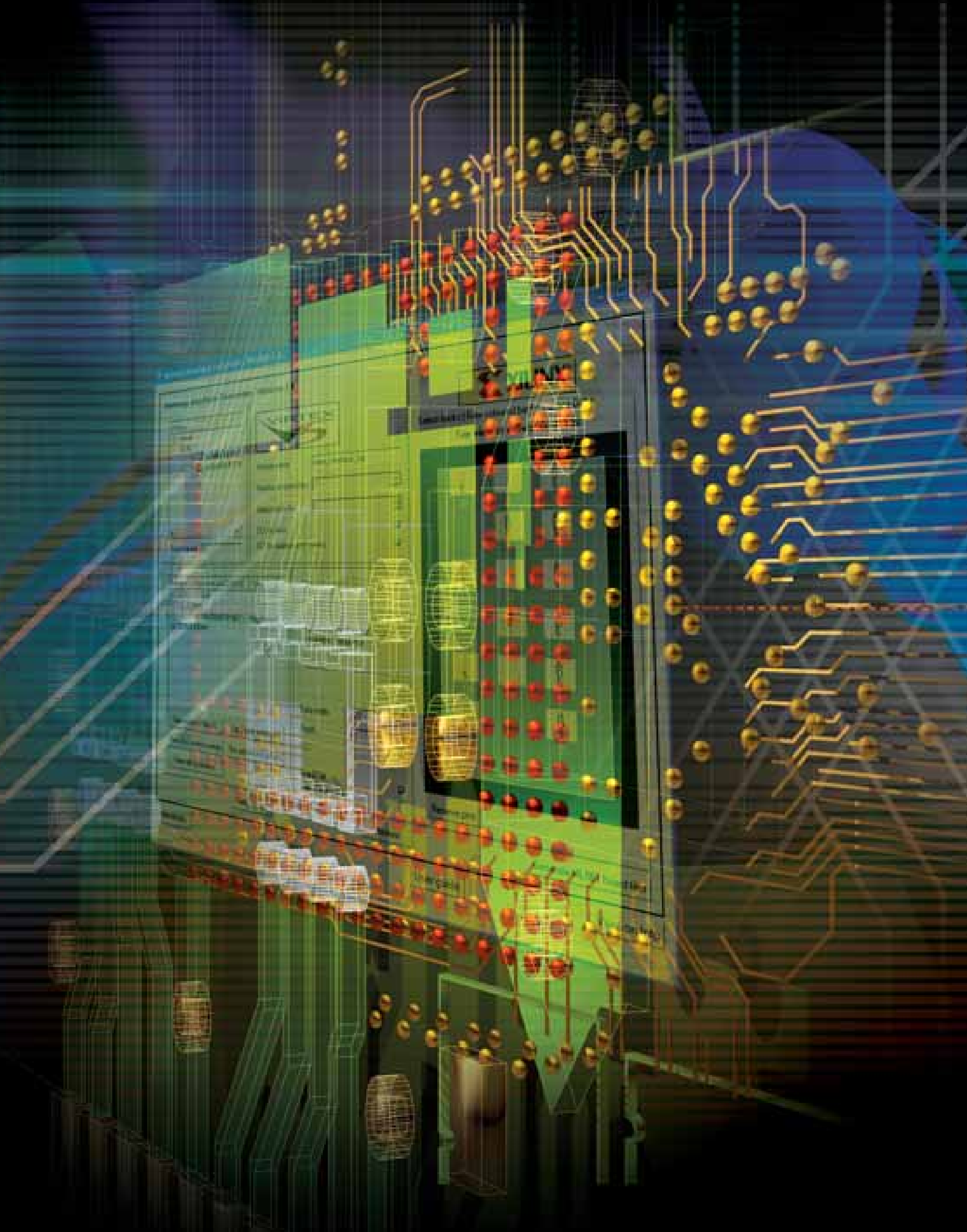
Implementing Memory Controllers Using the Memory Interface Generator Tool

The Memory Interface Generator tool simplifies designing memory controllers for Xilinx FPGAs.



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The Memory Interface Generator (MIG) tool is a comprehensive tool used to simplify the design of memory controllers for Xilinx® FPGAs. Memories are part of a majority of Xilinx applications. The goal of the MIG tool is to simplify memory interfaces, thus enabling FPGA users to focus on the rest of the system design.

The MIG tool was first introduced in 2002 as a memory controller pin selection utility for Virtex™-II and Virtex-II Pro FPGAs. Since then, the MIG tool has progressed significantly; it now supports all Xilinx FPGA devices, including Virtex-4, Virtex-5, Spartan™-3, and Spartan-3E FPGAs.

The MIG tool dynamically generates HDL in Verilog or VHDL formats based on user inputs. Additionally, the MIG tool generates .ucf pin constraints, any slice and logic placement constraints, and any other constraints required to create high-performance designs with minimal user changes.

MIG outputs are fully available in non-encrypted formats. This enables you to modify the designs.

The Time-to-Market Advantage

High speed memories are complex to design. Conservatively, you can save more than six months by using the targeted reference designs provided by the MIG tool.

Fully verified MIG reference designs enable you to focus on other design activities, thus reducing overall time to market.

MIG Controller Architecture

The MIG tool produces everything required to fully implement a memory controller. MIG controllers are implemented in logical layers comprising:

1. The physical layer, or PHY, which captures the read data, transfers it to a convenient clock domain, and stores it. The PHY also transmits the write data and command/control signals.
2. The controller generates the required commands based on user requests. The controller also implements the state machine for reading, writing, and refreshing the memory.
3. The user interface enables exchange of data and commands to and from your application.

This layered approach allows you to modify the required portions of the design. In Virtex-5 devices, Xilinx has further simplified the layering compared to previous designs. For example, some designers want to use their own controllers, which is possible by replacing the controller that the MIG tool generates. This is easily achieved in Virtex-5 designs.

Hardware Verification

The designs generated by the MIG tool are thoroughly verified to ensure high quality. These quality checks have increased significantly over time as we at Taray learn more from the field.

For a given FPGA family, we verify at least one set of designs in hardware. Hardware verification is usually performed on a Xilinx memory reference board, such as the ML461 or ML561 boards.

Hardware verification starts with a point test, such as a read/write data match, at a particular frequency for a given memory part. We then perform frequency sweeps and ensure that the designs work ±10% in the required frequency range. We also verify all the possible parameters such as column address strobe (CAS) latencies, burst lengths, and data widths, as well as all supported synthesis tools.

Simulations

Taray simulates MIG designs using ModelSim from Mentor Graphics. We simulate a large number of combina-

Hardware-Tested Configurations	
HDL	Verilog and VHDL
Synthesis Tools	XST and Synplicity
Board and FPGAs	ML 461 –> XC4VLX25-FF668-10 and ML 462 –> XC4VLX25-FF668-11
Burst Lengths	4 and 8
CAS Latencies	3 and 4
Additive Latencies	0, 1, and 2
ODT (in Ohms) Verified	0, 75, and 150
Depth Verified for Components	1
Depth Verified for DIMMs	1, 2, 3, and 4
Component Verified	MT47H32M16BT-37E
DIMM Verified	MT18HTF6472G-53E (Registered DIMM)
Component Data Width Verified	16
DIMM Data Width Verified	72 and 144
ECC Verified	72 and 144
Frequency Range	100 MHz to 280 MHz for 16-bit component 100 MHz to 250 MHz for 72-bit DIMM (with and without ECC) 100 MHz to 250 MHz for 144-bit DIMM (with and without ECC)
Simulation-Tested Configurations	
HDL	Verilog and VHDL
Burst Lengths	4 and 8
CAS Latencies	3 and 4
Additive Latencies	0, 1, and 2
ODT (in Ohms) Verified	0, 75, and 150
Depth Verified	1, 2, 3, and 4 (for both components and DIMMs)
Components Verified	All supported by the MIG tool (X4, X8, and X16)
DIMMs Verified	All supported by the MIG tool (registered, unbuffered, and SODIMMs)
Component Data Width Verified	8, 16, 24, 32, 40, 48, 56, 64, 72, 128, and 144
DIMM Data Width Verified	64, 72, 128, and 144
ECC Verified	40, 72, and 144
Frequencies Verified	200 MHz and 267 MHz (for both components and DIMMs)
Initialization	As per both Micron and JEDEC specifications
Multicontroller	1 to 8

Table 1 – Hardware and simulation test summary for Virtex-4 DDR2 SDRAM designs

tions and ensure that every memory listed in the MIG tool is verified with at least one of the test cases. Table 1 is a summary of the different simulation test cases for Virtex-4 DDR2 SDRAM designs. Below are some parameters to generate the test cases:

- All possible data widths
- All of the supported memory components/DIMMs
- Different values for CAS latencies, burst lengths, and additive latencies, depending on the memory type
- Simulated Verilog and VHDL RTL files
- RTL with and without testbench
- RTL with and without DCM
- Use memory models with different frequencies

Key Features

The MIG tool is part of Xilinx ISE™ software and is invoked through the CORE Generator™ tool. Figure 1 is a screen shot of the MIG GUI. The key features of the MIG tool v1.6 are:

- Virtex-5 FPGAs:
  - DDR2 SDRAM, Verilog
  - QDR II SRAM, Verilog
- Support for Virtex-4 FPGAs (and the following designs):
  - DDR2 SDRAM, Verilog and VHDL, direct clocking
  - DDR SDRAM, Verilog and VHDL, direct clocking
  - QDR II SRAM, DDR II SRAM, Verilog and VHDL, direct clocking
  - RLDRAM II, Verilog and VHDL, direct clocking
  - DDR2 SDRAM, Verilog and VHDL, SERDES clocking
  - All Virtex-4 designs support both XST and Synplicity
- Spartan-3 FPGAs:
  - DDR SDRAM, Verilog and VHDL
  - DDR2 SDRAM, Verilog and VHDL
- Spartan-3E FPGAs:
  - DDR SDRAM, Verilog and VHDL
  - All Spartan-3 and Spartan-3E designs support XST, Synplicity, and Precision Synthesis
- Support for many different memory components and DIMMs
- Pins picked are based on the selected memory part and user inputs
- Generates RTL and bit files for Xilinx reference boards containing memories
- Basic I/O design rule check (DRC) engine ensures that signals are allocated correctly
- Verifying a modified MIG .ucf file ensures that MIG pin-out rules are valid

Using the Outputs of the MIG tool

The MIG tool generates everything required to create a memory interface:

- The RTL (Verilog or VHDL) design files
- Synthesis scripts
- ISE scripts for build, map, and place and route
- A .ucf file for pin locations, RLOCs, and any other constraints

After generating the design RTL, you can execute a batch file to synthesize, map, and place the design. The MIG tool generates two designs – one with a testbench and another without. The MIG scripts work on the version with the synthesizable testbench. However, you can integrate your applications to the version without the testbench.

Conclusion

The MIG tool significantly reduces design burden and improves time to market. It has been used successfully by many customers.

For a copy of the Memory Interface Generator or for additional information, visit *www.xilinx.com/memory*.

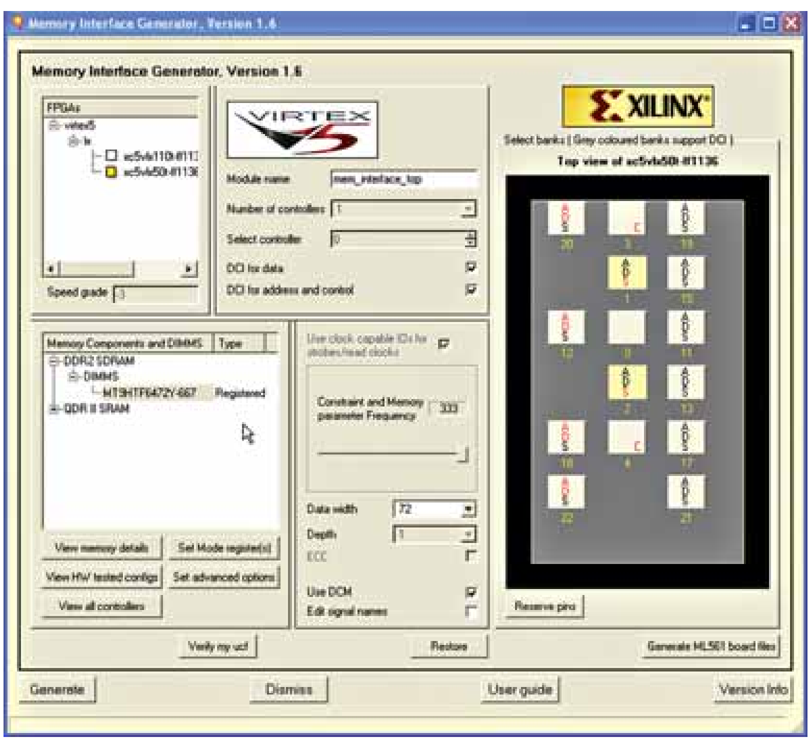

Figure 1 – The MIG tool 1.6 GUI