

# Designing Virtex-5 DDR2 Memory Interfaces for Signal Integrity

Follow these guidelines to make your next Virtex-5 DDR2 design experience a success.

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Let's say that you are about to design your first Xilinx® Virtex™-5 DDR2 memory interface. You need quick guidelines for preferred circuit topologies and a quick summary of the trade-offs involved when using digitally controlled impedance (DCI) on-die termination instead of external termination resistors. In this article, I'll provide practical design guidelines taken from previous real-world design experience, as well as IBIS simulation results.

## Circuit Topologies for Memory Interfaces

Figures 1 and 2 show several possible topologies for DDR2 address/control and data lines, respectively. On the bidirectional data lines, I made the memory chip the driver and the Virtex-5 device the receiver to make use of the FPGA's DCI. The top schematic diagram in Figure 1 shows the preferred and recommended use model, while the other diagrams show variations often tried in regular design practice.

Figures 3 and 4 show typical receiver eye diagrams corresponding to the topologies shown in Figures 1 and 2, respectively. The input switching thresholds of the receiver are shown as horizontal dashed blue lines for reference. The color of the “probe” arrows in Figures 1 and 2 correspond to the colors of the associated traces in Figures 3 and 4, respectively. I used Mentor Graphics’s HyperLynx software to generate these eye diagrams with the following parameter settings:

- Pseudo-random binary sequence (PRBS) with bit order 7 (a sequence length of 127)

- Bit interval = 1.5 ns (667 Mbps)
- One sequence repetition
- First 50 bits skipped
- Zero added jitter

When looking at the traces in Figure 3, it should be obvious that of the three topologies shown, the recommended use model gives by far the cleanest eye.

The middle schematic in Figure 1 shows a typical mistake made by novice DCI users, which is to assume that using SSTL18\_I\_DCI drivers eliminates the need for any external termination components. Some DCI users often incorrectly

assume that the “\_DCI” versions of the SSTL (stub series terminated logic) driver family adjust their output impedance to match the DCI calibration resistors and can therefore be used as matched impedance drivers of the transmission line.

But this is not true. The SSTL18\_I\_DCI output driver, for instance, has a fixed output impedance of approximately 20Ω, as per the SSTL18 specification. The disastrous results of this erroneous assumption are clearly visible in the yellow trace shown in Figure 3. Not only has the eye been drastically narrowed, but problematic overshoot/undershoot has also been introduced at the receiver input.

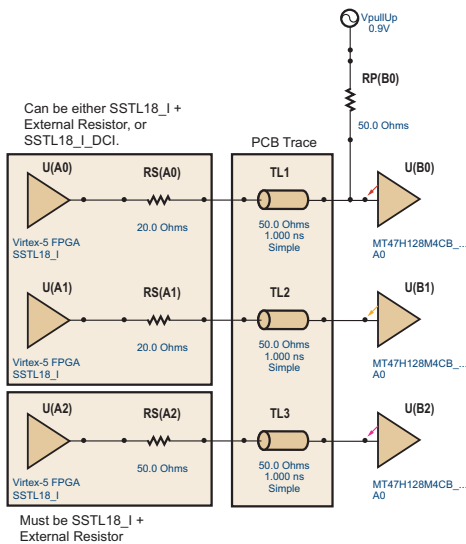


Figure 1 – Typical address/control circuit topology

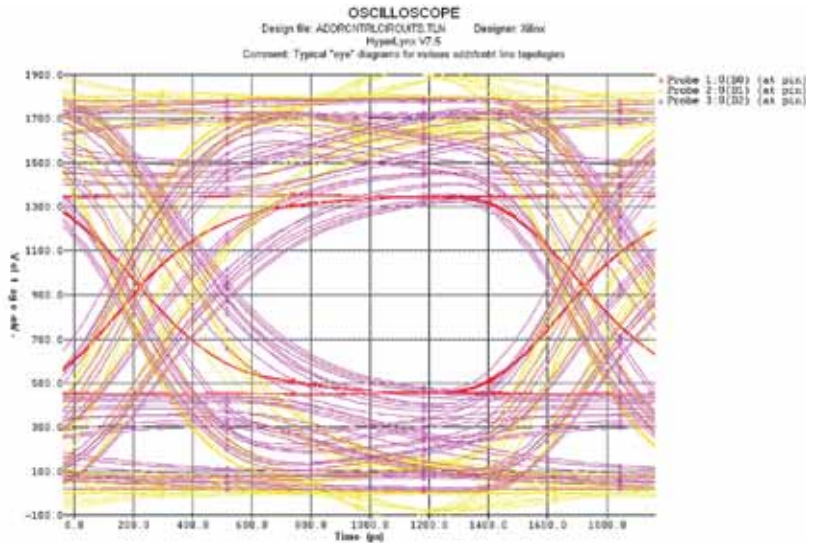


Figure 3 – Typical eye patterns for address/control

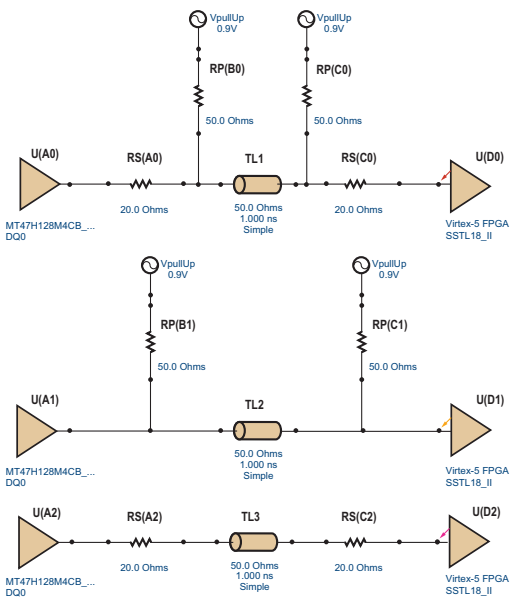


Figure 2 – Typical data circuit topology

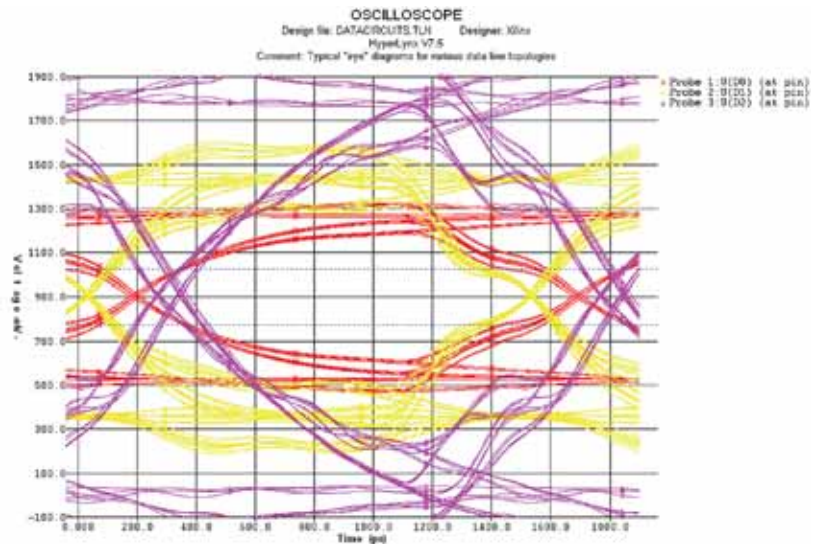


Figure 4 – Typical eye patterns for data

## ...blindly following recommended use models, rules of thumb, or general guidelines is never a good substitute for simulating your design.

Increasing the series termination to  $50\Omega$ , as shown in the bottom schematic in Figure 1, successfully eliminates overshoot/undershoot but does nothing to restore the eye to its original width. Therefore, you should always use parallel termination at the end of all address/control lines.

If an appropriate termination voltage source is not available, you can form a Thevenin-equivalent termination using two resistors connected in series between the  $V_{CCO}$  supply and ground, where each resistor has a value twice that of the desired impedance. In this case, simply terminate the line by connecting its end point to the net that connects the two resistors. Note that your circuit consumes more power when terminated in this fashion because of the constant load on the  $V_{CCO}$  supply formed by the two resistors.

The data-line eyes in Figure 4 also illustrate that removing the parallel termination from the ends of the line causes unacceptable overshoot/undershoot. However, in this case, removing the series terminations appears to have improved the eye, making it slightly wider and providing more “head room” against noise without introducing overshoot/undershoot. This serves as an excellent reminder that blindly following recommended use models, rules of thumb, or general guidelines is never a good substitute for simulating your design.

Keep in mind that before approving an engineering change order (ECO) for the removal of the series termination resistors, you should reverse the direction of the line with the Virtex-5 device driving data to the memory chip and check the eye for good signal integrity (SI).

### Why Use DCI?

The benefits of using DCI, as opposed to equivalent external termination, are numerous, including:

- Better SI at receiver inputs
- Reduced PCB size

- Reduced bill of materials (BOM) parts count

SI at receiver inputs improves when using DCI because the termination lies closer to the inputs than when you use an external termination resistor.

PCB size and BOM parts count are both reduced when using DCI because of the elimination of external termination components.

Caveats when using DCI include:

- Impedance variation over process/voltage/temperature
- Greater power consumption

The termination impedance when using DCI is provided by CMOS transistors; therefore, the value of that impedance can vary along with variations in the fabrication process, supply voltage, and operating temperature (PVT) of the FPGA. You should always perform system-level SI simulations twice, using the high and low extremes for the value of the termination impedance to ensure correct system operation across all possible combinations of PVT.

Using DCI for parallel termination at the end of a transmission line results in higher power consumption than using an external resistor, assuming that an appropriate termination voltage source is available. In this case, the end of the line can be connected to the voltage source through a resistor with a value equal to the characteristic impedance of the line, and no load will be placed across the supply rails.

Conversely, when DCI is used to terminate the line, two pass transistors connect the receiver input to  $V_{CCO}$  and ground, respectively. Each transistor is adjusted to have an effective resistance equal to twice the characteristic impedance of the line, thus producing a Thevenin-equivalent termination impedance of  $Z_0$  to  $V_{CCO}/2$ .

A side effect of this termination scheme is that an additional load of  $4Z_0$  appears

across the supply rails, consequently increasing overall system power consumption. If the system architectural design specifications do not provide for a voltage supply at  $V_{CCO}/2$ , then no power penalty is incurred for using DCI because the termination scheme has to be Thevenin-equivalent in either case.

Table 1 gives the worst-case output power dissipation of a single line for three termination styles: source series, external parallel (assuming availability of  $V_{CCO}/2$ ), and internal parallel (DCI).

| Termination Type                    | Power Dissipation |
|-------------------------------------|-------------------|
| External Source Series Termination  | 41 mW             |
| External Parallel Termination       | 49 mW             |
| Internal (DCI) Parallel Termination | 57 mW             |

Table 1 – Power dissipation versus termination type (for a discussion of output power calculations, see “High-Speed Digital Design: A Handbook of Black Magic” by Howard Johnson and Martin Graham)

### Conclusion

In this article, I’ve shown how various digressions from the Xilinx recommended use model for circuit topology of DDR2 memory interfaces affect the eye at the receiver. I hope you are convinced that system-level simulation with an IBIS simulator such as HyperLynx is a necessity when designing DDR2 memory interfaces. And I’ve given you some pros and cons for using DCI as an alternative to external termination resistors in your next DDR2 design.

Going forward, as memory interface speeds continue to increase and I/O voltage levels continue to decrease, you will be able to apply the general principles learned here to the design of more complex memory interfaces as those standards emerge.

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