

Improve System Reliability with SPI-4.2 LogiCORE Solutions and Virtex-5 FPGAs

Virtex-5 devices provide an ideal platform for source-synchronous designs like the widely adopted SPI-4.2 interface.

by Dean Armintrout
Product Marketing Engineer, IP Solutions Division
Xilinx Inc.
dean.armintrout@xilinx.com

Chris Ebeling
Principal Engineer, IP Solutions Division
Xilinx, Inc.
chris.ebeling@xilinx.com

System Packet Interface Level 4 Phase 2 (SPI-4.2) is the Optical Internetworking Forum's recommended interface for the interconnection of devices for aggregate bandwidths of OC-192 (ATM and POS) and 10 Gbps (Ethernet), as illustrated in Figure 1.

The SPI-4.2 interface has become the standard for interconnecting leading-edge 10 Gbps framers, traffic managers, network processors, and switch fabrics. SPI-4.2 is popular because of its efficient interface, which offers high bandwidth and low pin count, along with seamless handling of typical system requirements such as flow control, error detection, synchronization, and bus realignment.

The Xilinx® Virtex™-5 architecture provides an ideal platform for implementing SPI-4.2. The Xilinx SPI-4.2 LogiCORE™ IP targeting Virtex-5 devices provides a significantly smaller solution with dramatic power savings, 1.2 Gbps LVDS DDR I/O, and complete pin assignment flexibility.

SPI-4.2 LogiCORE IP

Continually improving on its SPI-4.2 solution, Xilinx has made the latest implementation 25% smaller than previous versions by leveraging the 65-nm ExpressFabric™ technology and real six-input look-up tables (LUTs) of Virtex-5 FPGAs.

Enhanced ChipSync™ technology is supported on every pin of the Virtex-5 device family, allowing you to target the SPI-4.2 LogiCORE solution to any device pinout to meet your system and PCB requirements. High-performance interfaces are supported by 1.2 Gbps LVDS data rates.

For applications requiring multiple SPI-4.2 interfaces, the Virtex-5 FPGA's logic density, high pin count, and extensive clocking resources support four or more full-duplex cores in a single device.

ChipSync Source-Synchronous Technology
Virtex-5 devices build on ChipSync technology to ensure reliable high-speed data transfer for source-synchronous applications like SPI-4.2 with these features:

- Built-in serializer/deserializer (SERDES) logic enables the fabric to interface to the I/O at a fraction of the source-synchronous clock rate. The included bit-slip function allows shifting of the deserialized data to achieve word alignment when linking multiple pins (bus deskew).
- Input delay (IDELAY) components allow the dynamic phase alignment (DPA) logic to independently adjust the delay of each bit of a bus in 75-ps increments, providing a mechanism for tuning the interface timing to the system environment.
- DDR registers integrated into the I/O pins simplify the interface between the FPGA fabric and the I/O blocks by supporting data transfer on a single clock edge.

SPI-4.2 and ChipSync Technology

The SPI-4.2 interface has a DDR source-synchronous data bus that comprises 18 LVDS pairs (16 data, 1 control, and 1 clock), operating at a minimum rate of 311 MHz.

The SPI-4.2 core uses ChipSync technology to serialize/deserialize bus data to a four-word SPI-4.2 datastream at a lower clock rate; thus, you can implement high-frequency SPI-4.2 interfaces in slower speed grade Virtex-5 devices.

The SERDES functions allow the core logic to transfer these four words to and from the I/O logic without using any CLB logic resources and operate at half the source-synchronous DDR clock rate. For example, a SPI-4.2 interface with a 500-MHz DDR reference clock only requires an FPGA fabric clock of 250 MHz – easily achievable in the Virtex-5 architecture.

As the frequency of the source-synchronous clock increases, data recovery at the receiving (sink) device becomes more challenging. The SPI-4.2 protocol provides a training pattern that permits a receiving device to adjust its data sampling to the sys-

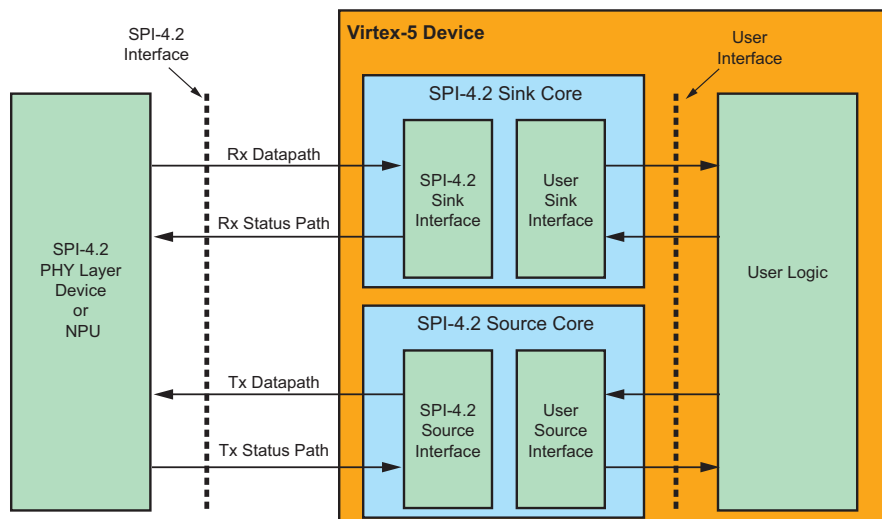


Figure 1 – Typical SPI-4.2 application

tem interface timing – a process referred to as dynamic phase alignment (DPA).

In Virtex-5 FPGAs, the IDELAY feature present in every I/O is ideally suited to adjust the clock-data phase relationship for maximum I/O timing margin. This has two primary benefits for the SPI-4.2 core:

- Integrating the IDELAY feature into the input pin (ILOGIC) reduces the FPGA resources required for DPA to less than 350 slices.
- The IDELAY function’s ability to adjust the data sampling point enables DPA to be implemented in the I/O – except for a small control state machine implemented in the fabric. The state machine portion is fully synchronous and does not require a complex macro. Thus, there are no restrictions on SPI-4.2 pin assignments.

Continuous DPA

The Xilinx SPI-4.2 LogiCORE solution enhances communication system reliability with continuous DPA, which monitors the clock-data alignment during operation and constantly adjusts the data sampling points to adapt to system timing changes.

Following the initial clock-data alignment phase, the sampling point of each data bit is aligned to the middle of the data valid window (Figure 2a). This window can

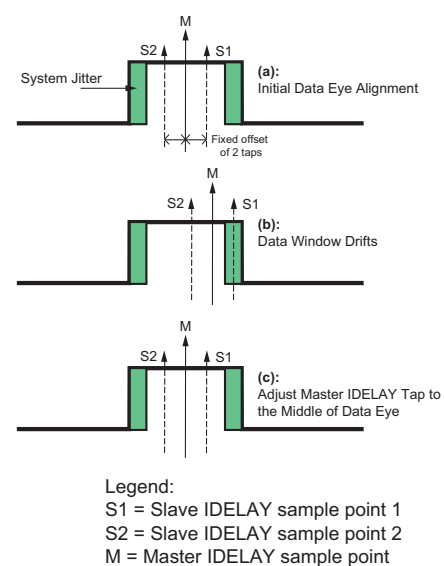


Figure 2 – Continuous DPA operation

shift with changes in operating conditions, such as voltage and temperature, as well as other variations (Figure 2b). Continuous DPA addresses this by constantly monitoring the ingress data and adjusting the sample point of each data bit to provide the maximum timing margin (Figure 2c).

Although the OIF SPI-4.2 Implementation Agreement calls for the insertion of periodic training patterns to maintain clock-data alignment over time, Xilinx continuous DPA does not depend on the presence of training patterns. By

reducing/eliminating the need for periodic training patterns, continuous DPA enables the maximum data bandwidth in your system while maintaining the optimal clock-data alignment at each pin.

DPA Diagnostics

If your hardware operation encounters alignment issues, the Xilinx SPI-4.2 core includes DPA diagnostic ports to aid with debugging. The DPA diagnostic data monitors the data eye and final sampling point of the initial alignment process, as well as a second sweep of the data valid window to determine if any changes have occurred.

You can connect the diagnostic ports to the ChipScope™ analyzer or other logic probes to analyze alignment conditions while the FPGA is on the board, interacting with the rest of the system



Figure 3 – Illustration of four instances of SPI-4.2 LogiCORE IP implemented on a Virtex-5 XC5VLX110 device

Clocking Resources

Virtex-5 FPGAs provide an unprecedented number of clock resources for implementing multiple SPI-4.2 interfaces in a single device. The abundance and flexibility of clock distribution in the Virtex-5 family solves this challenge, supporting as many SPI-4.2 interfaces as the device logic and I/O will accommodate.

In the Virtex-5 family, all devices have 32 global clock resources, with any 10 of

	Virtex-4 FPGA	Virtex-5 FPGA
Power: Static Alignment @ 700 Mbps per LVDS Pair	1.55W	1.42W
Power: Dynamic Alignment Performance per LVDS Pair	2.0W @ 1 Gbps	1.66W @ 1 Gbps
Speed Grades Supporting 800 Mbps per LVDS Pair	-10, -11, -12	-1, -2, -3

Table 1 – SPI-4.2 power estimates for Virtex-4 and Virtex-5 FPGAs

the 32 total global buffers available in each clock region. The global clock trees and associated buffers are implemented differentially for best duty-cycle fidelity and greater common-mode noise rejection.

In addition, each region in the device has four regional clock nets, which are ideal for source-synchronous interface clocking at rates above 1 Gbps. You can configure the SPI-4.2 LogiCORE IP to use either global or regional clock resources.

These high-performance clock resources support as many as four SPI-4.2 interfaces in a mid-range device (LX85/LX110) and more than four SPI-4.2 interfaces in the larger devices (Figure 3). The Virtex-5 clocking capability enables a whole new class of SPI-4.2 applications and provides an ideal platform for applications such as multiplexing and demultiplexing, bridges, and switches.

Higher Performance at Lower Power

Virtex-5 silicon is manufactured with a 65-nm triple-oxide process that reduces power consumption by as much as 35%. This has a positive impact for all designs, including the SPI-4.2 interface; the power savings are summarized in Table 1.

With Virtex-5 devices, SPI-4.2 uses significantly less power than its predecessors, both because of the enhanced 65-nm process and because the LogiCORE solu-

tion uses 25% less fabric resources. At the same time, Virtex-5 FPGAs support 20% higher performance for SPI-4.2, with high-speed 1.2 Gbps LVDS data rates on every I/O of the device.

This means that not only can you place multiple SPI-4.2 interfaces anywhere on the device, but for each interface, you can realize an aggregate bandwidth as high as 19 Gbps. Designs not requiring this level of performance (such as more typical framer interfaces

running at 10-12 Gbps) automatically get additional performance overhead, ensuring ease of design integration and timing closure.

Conclusion

Xilinx SPI-4.2 LogiCORE IP coupled with Virtex-5 features provides a highly efficient and reliable SPI-4.2 solution. We developed ChipSync technology and continuous DPA specifically for source-synchronous interfaces like SPI-4.2.

This technology allows you to design the most efficient and reliable SPI-4.2 solutions, which use significantly less resources (25% less), allow fully flexible device pin assignments (you choose the pinout), and support extremely high interface speeds (1.2 Gbps LVDS DDR I/O).

The higher performance is even more remarkable because Virtex-5 FPGAs achieve this while consuming significantly less power. The wealth of Virtex-5 clocking resources, combined with full pin assignment flexibility, enables a new class of applications with multiple SPI-4.2 interfaces.

For more information about the SPI-4.2 LogiCORE IP targeting Virtex-5 devices, visit the Xilinx IP Center at www.xilinx.com/systemio/spi-4.2. A hardware demonstration is also available; for more information, contact your Xilinx representative. ●●●