

Tackling Serial Backplane Interface Design Challenges

The Virtex-5 LXT FPGA enables robust, high-performance, and high-integration serial backplane interface solutions.

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The rate of adoption of serial technology in high-end system design has reached critical mass. As shown in Figure 1, 92% of respondents in a recent *EE Times* survey answered “yes” when asked if they were designing serial I/O systems in 2006, compared to 64% serial design activity in 2005.

A good portion of this dramatic adoption rate is caused by the penetration of serial technology in backplane applications. As system throughput requirements increase, the parallel backplane technologies of old will be displaced by SerDes-based backplane subsystems that provide higher bandwidth, better signal integrity, lower EMI and power, and simpler PCB designs.

Further promoting this growth is the emergence of standard serial protocols such as XAUI and Gigabit Ethernet (GbE),

which allow reduced engineering efforts and interoperability. Standardization efforts for serial backplane form factors such as AdvancedTCA and MicroTCA in the PCI Industrial Computer Manufacturers Group (PICMG) have also contributed to the accelerated adoption. The benefits of serial backplanes are so compelling that they have been used as the backbone of not only communications, compute, and storage systems but also broadcast, medical, defense, and industrial/test systems.

Persistent Design Challenges

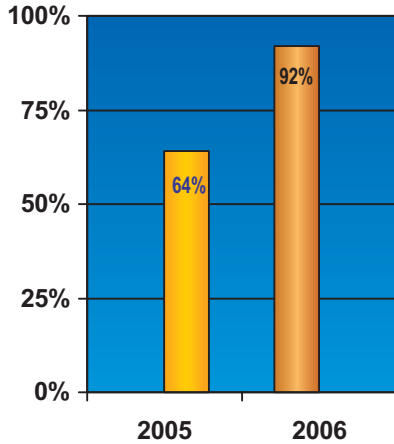
Regardless of the increased rate of adoption, many design challenges still exist. Because the backplane subsystem is the heart of the system, it must be able to pass signals from card to card reliably. Thus, designing backplanes with high signal integrity (SI) is of primary importance.

Also significant is the use of proper silicon ICs with SerDes technology, capable of driving backplanes with very

low bit-error rates. Silicon-based approaches to mitigating SI issues are particularly important in “legacy upgrade” scenarios, in which designers re-use older backplanes with legacy components and design rules.

There are also challenges in developing serial backplane protocols and fabric interfaces. The majority of backplane designs leverage legacy ASICs, which have proprietary protocols. Even some newer backplane designs require a proprietary backplane protocol. Silicon solutions must therefore be flexible and provide the necessary customizability. Although an ASIC allows this, it can often be costly and risky, with unproven product demand/volume and the possibility of design bugs and specification changes.

An approach that has recently gained traction is the use of off-the-shelf standards-based switch fabrics. This saves development time, but you must have silicon solutions that conform to the standard



Source: EE Times Survey, 2005

Figure 1 – Percentage of engineers designing Serial I/O systems

protocol, as well as the flexibility to customize the end product and make it unique.

And of course, there are the ever-present challenges of cost, power, and time to market. To meet the challenges of serial backplane design, Xilinx provides the Virtex™-5 LXT platform of FPGAs as well as IP solutions.

Xilinx Solutions for Serial Backplanes

The key technology that enables the application of Xilinx® Virtex-5 LXT FPGAs in serial backplane applications is the embedded RocketIO™ GTP low-power serial transceiver. There are as many as 24 serial transceivers in the largest Virtex-5 LXT FPGA; each serial transceiver is capable of running from 100 Mbps to 3.2 Gbps. Coupled with programmable fabric, the FPGA is capable of supporting virtually any serial protocol – proprietary or standard – up to 3.2 Gbps.

More important for serial backplane applications are built-in signal conditioning features, including transmit pre-emphasis and receive equalization. These features enable transmission of multi-gigabit signals over long distances, often reaching 40 inches or longer. Both equalization methods minimize the impact of inter-symbol interference (ISI) by boosting high-frequency signal components and attenuating low-frequency components. The difference is that pre-emphasis is performed on the transmitted signal as

it goes out of the line driver, while equalization occurs on the received signal after it enters the IC package. Both pre-emphasis and equalization features are programmable to different states to allow for optimum signal compensation.

Besides signal conditioning features, the serial transceivers also provide additional features beneficial for backplanes, such as programmable output swings that allow interfacing to a variety of other current mode logic (CML)-based devices and built-in AC coupling capacitors that simplify transmission line design and reduce ISI.

IP Cores

Proprietary protocols still make up most serial backplane implementations. However, some newer designs have used standards-based protocols such as XAUI and GbE. This growing acceptance has been driven primarily by the maturity of these standards and the emergence of switch fabric ASSPs utilizing these protocols. Using ASSPs for switching applications saves tremendous development time, but designers realize that they need to differentiate their products by adding value-added capabilities, primarily on the line card.

FPGAs are the ideal platform for providing customizability, as the serial transceivers are designed to support a majority of standard serial backplane protocols. Together, the serial transceivers and fabric allow for standards-compliant designs with value-added functions – all in a single silicon device.

To reduce design time, Xilinx offers off-the-shelf available IP cores for key serial I/O interface standards such as XAUI, GbE, SRIO, and PCIe. To ensure interoperability,

these IP cores are tested through consortia plug-fests and independent third-party verification. To facilitate the creation of lightweight serial protocol designs, Xilinx also created the Aurora protocol, which is ideal for simpler designs requiring minimal overhead and optimized slice/resource utilization.

With increased usage of Ethernet and PCIe, Virtex-5 LXT FPGAs also include embedded tri-mode Ethernet MACs and PCIe Endpoint blocks. These allow significant savings of FPGA slice resources for customers needing interfaces in control plane applications, for example.

Because many chips with parallel interfaces are still used even in newer systems, Xilinx also offers IP cores for popular parallel interfaces such as SPI-4.2, SPI-3, and PCI. These allow you to rapidly create serial-to-parallel bridges, which are still required in many applications.

Besides serial and parallel interface IP, Xilinx offers more complete IP solutions that further reduce development time and time to market. These solutions include a Traffic Manager for prioritizing traffic flows across backplanes, as well as a Mesh Fabric Reference Design that allows “every-to-every” connectivity between cards. Lastly, the ChipScope™ Pro Serial I/O Tool Kit enables rapid serial transceiver setup and debugging as well as BERT testing. Table 1 summarizes the serial backplane-related IP available from Xilinx.

Application Examples

Let’s look at how you could integrate all of the solution components to create a complete serial backplane fabric interface FPGA for both a star and mesh system.

IP Category	Available IP
Serial Interfaces	XAUI, GbE, PCI Express, Serial RapidIO, Aurora, CPRI, OBSAI
Parallel Interfaces	SPI-4.2, SPI-3, Utopia, PCI, CSIX
System-Level Solutions	10G Traffic Manager, Mesh Fabric Reference Design
Serial Backplane Test Solutions	ChipScope Pro Serial I/O Tool Kit

Table 1 – Xilinx IP for serial backplanes

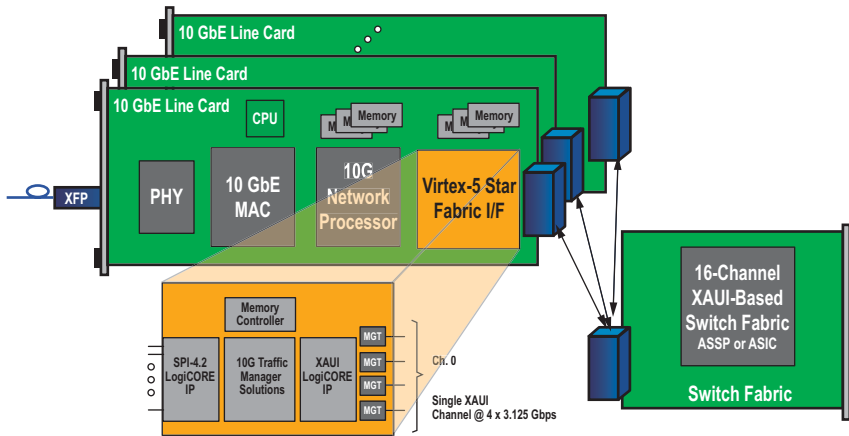


Figure 2 – Star fabric I/F FPGA in a 10 GbE line card

which requires full connectivity between four 24-port VDSL line cards and a 10 GbE backhaul card that connects to a metro Ethernet network. Each card uses a Virtex-5 LXT device and four embedded serial transceivers to realize the four independent channels of the mesh fabric physical layer. Implementing the four link layers is the Aurora protocol, which runs at approximately 3 Gbps to transport the 2.4 Gbps payload – plus additional overhead such as the encoding.

A SPI-4.2 and SPI-3 LogiCORE IP is used on the trunk card and line cards, respectively, providing connectivity to the network processor. The Mesh Fabric Reference Design and Traffic Manager solution provide the distributed switching and QoS functions required on all of the line cards.

The line card fabric interface could easily fit in an XC5VLX30T device, while the trunk card fabric could fit in an XC5VLX50T device. Similar to the star example, you can realize significant benefits in integration, time-to-market reduction, feature optimization, and power and cost reduction by using the Virtex-5 LXT solution.

Conclusion

Serial backplane technology is now mainstream; its adoption will only continue to increase with the rapidly growing demand for bandwidth. Evolution of backplane system requirements in terms of rates and protocols is inevitable and designers will face new challenges.

However, with Xilinx Virtex-5 LXT FPGAs and off-the-shelf-available IP for serial backplanes, system architects have an option that can accommodate legacy as well as newer backplane designs. Virtex-5 LXT FPGAs with embedded SerDes have the critical SI-improving features and integration required to provide high reliability and area- and cost-optimized designs.

Furthermore, Xilinx off-the-shelf IP reduces development time and time to market. Together, the powerful silicon and IP cores are what make the Virtex-5 solution the ideal vehicle for tackling even the toughest serial backplane design challenge.

For more information, visit www.xilinx.com/backplanes and www.xilinx.com/qos.

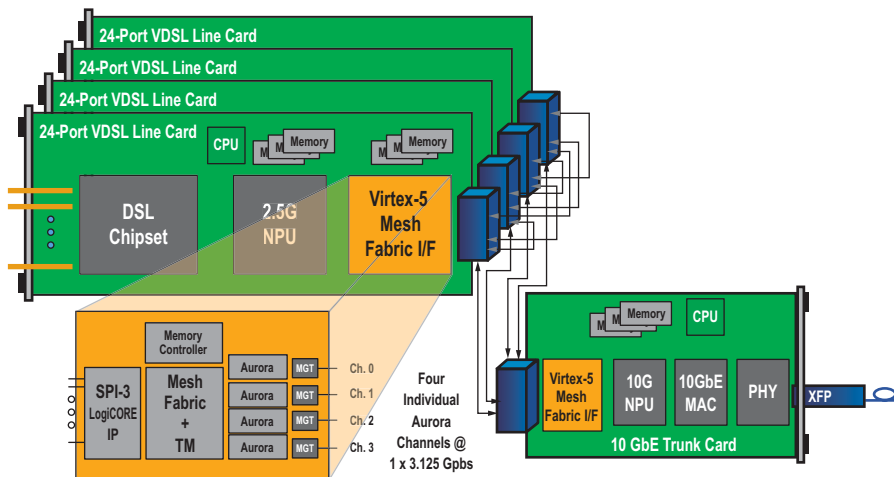


Figure 3 – Mesh fabric I/F FPGA in a VDSL line card

Star Backplane Topology Application

Star fabric topologies prevail in high-end infrastructure equipment because of their cost-effectiveness, particularly in systems with a high number of cards. Figure 2 is an example of a 10 GbE line card that implements an FPGA-based star fabric interface. This FPGA instantiates the XAUI LogiCORE™ IP and uses four serial transceivers to connect to the 16-channel XAUI switch fabric card. A LogiCORE SPI-4.2 core is also realized in the FPGA to interface to the 10 Gbps network processing unit.

Between the serial and parallel interface is the Traffic Manager IP, which performs QoS-related functions on ingress and egress traffic. A memory controller controls

the external memory, which is used primarily as packet buffers. The benefits of this architecture include increased integration of SerDes and logic functions and quick time to market through the use of IP, while allowing an implementation that meets your exact system specifications. It also provides solid SI as well as low SerDes power consumption (~400 mW total). You can implement all of this in the lowest cost speed grade XC5VLX50T device.

Mesh Fabric Architectures

Star topologies prevail in most cases, but in some smaller systems, a mesh topology is required. Take the case of the five-slot IP DSL access multiplexer shown in Figure 3,