



# Connectivity Solutions

Realize the full potential of the solutions in our silicon with Xilinx application notes.

## Memory Interfaces

### XAPP851 – DDR SDRAM Controller Using Virtex-5 FPGA Devices

By Toshihiko Moriyama and Rich Chiu

This application note describes a 200-MHz DDR SDRAM memory controller implemented in a Virtex™-5 device. This reference design uses the Virtex-5 ChipSync™ features to calibrate and adjust read data timing.

A straightforward back-end user interface is provided to allow integration into a complete FPGA design.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp851.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp851.pdf)

### XAPP852 – Synthesizable CIO DDR RLDRAM II Controller for Virtex-5 FPGAs

By Benoit Payette and Rodrigo Angel

This application note describes how to use a Virtex-5 device to interface to common I/O (CIO) double data rate (DDR) reduced latency DRAM (RLDRAM II) devices. The reference design targets two CIO DDR RLDRAM II devices at a clock rate of 200/300 MHz, with data transfers at 400/600 Mbps per pin.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp852.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp852.pdf)

### XAPP853 – QDR II SRAM Interface for Virtex-5 Devices

By Lakshmi Gopalakrishnan

This application note describes the implementation and timing details of a four-word-burst quad data rate (QDR II) SRAM interface for Virtex-5 devices. The synthesizable reference design leverages the unique I/O and clocking capabilities of the Virtex-5 family to achieve performance

levels of 300 MHz (600 Mbps), resulting in an aggregate throughput for each 36-bit memory interface of 43.2 Gbps.

The design greatly simplifies the task of read data capture within the FPGA while minimizing the number of resources used. A straightforward user interface is provided to allow simple integration into a complete FPGA design utilizing one or more QDR II interfaces.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp853.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp853.pdf)

### XAPP858 – High-Performance DDR2 SDRAM Interface in Virtex-5 Devices

by Karthi Palanisamy and Maria George

This application note describes the controller and data capture technique for high-performance DDR2 SDRAM interfaces. This data capture technique uses the input serializer/deserializer (ISERDES) and output double data rate (ODDR) features available in every Virtex-5 I/O.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp858.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp858.pdf)

## Source-Synchronous Interfaces

### XAPP855 – 16-Channel DDR LVDS Interface with Per-Channel Alignment

by Greg Burton

This application note describes a 16-channel source-synchronous DDR LVDS interface. The design takes advantage of the Virtex-5 I/O ChipSync feature's ability to adjust the delay of the receiver datapaths, creating dynamic setup and hold timing for each device at initialization and compensating for skews associated with the manufacturing process. The receiver operates at 1:8 deserialization on each of the 16 data channels.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp855.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp855.pdf)

### XAPP860 – 16-Channel DDR LVDS Interface with Real-Time Window Monitoring

by Greg Burton

This application note describes a 16-channel source-synchronous DDR LVDS interface. The receiver operates at 1:6 deserialization on each of the 16 data channels. Similar to XAPP855, the design also includes a real-time window monitoring circuit for added performance. This reference design calibrates and compensates for skews associated with process, voltage, and temperature (PVT) at initialization and also dynamically during operation.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp860.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp860.pdf)

## Serial Connectivity

### XAPP861 – Efficient 8x Oversampling Asynchronous Serial Data Recovery Using IDELAY

by John Snow

Virtex-5 devices have a high-precision programmable delay element (IDELAY) associated with every input pin. This application note shows how to implement 8x oversampling of many data streams using a single DCM, two global clock resources, and minimal FPGA logic resources. This solution provides better jitter tolerance than techniques using multiple DCMs. When paired with a suitable data recovery scheme, this oversampling technique can be used with many different data protocols up to 550 Mbps. A reference design is included that implements a SD-SDI (SMPTE 259M) receiver running at 270 Mbps.

On the Web at [www.xilinx.com/bvdocs/appnotes/xapp861.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp861.pdf)