



Designing Digital Displays with Spartan-3 Generation FPGAs

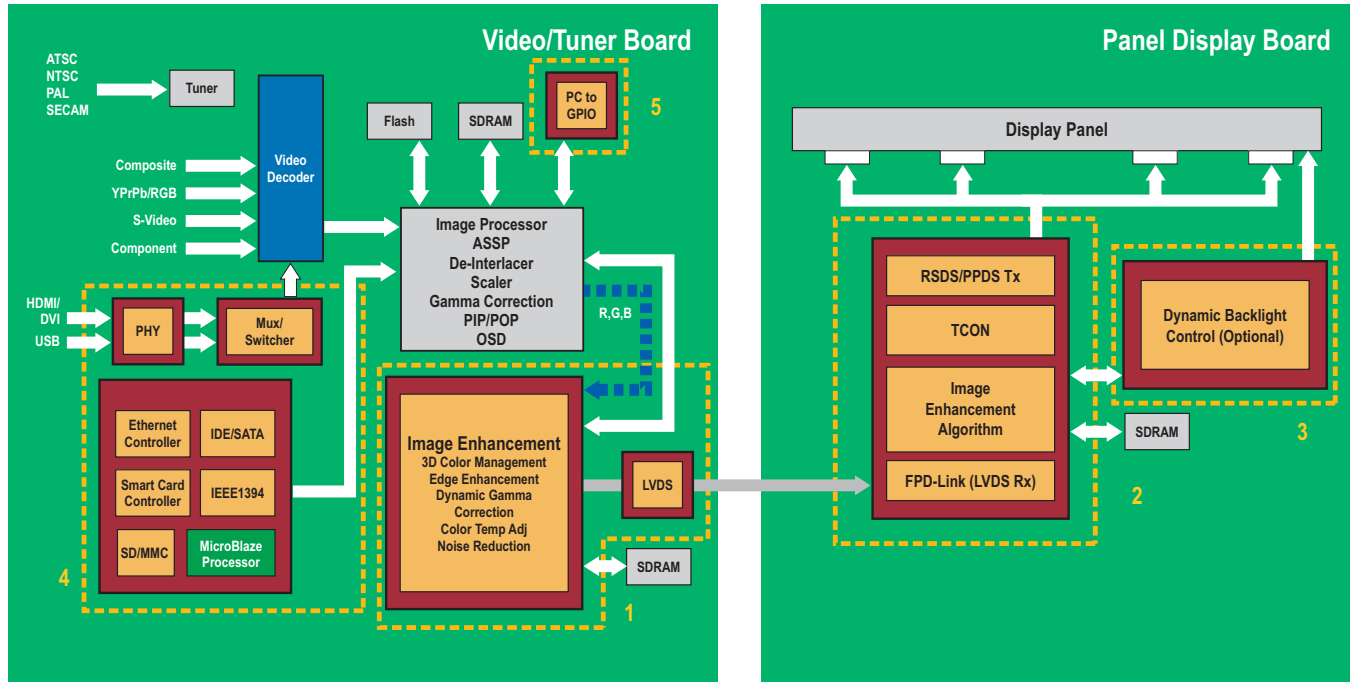
Programmable solutions improve your time to market.



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The dynamics of the digital display market to constantly strive for improvement while reducing total system cost has caused models to change between two to four times per year. These changes can be challenging as displays evolve; incorporating the right feature set in a very short time to market (TTM) becomes the standard business model to lead the pack or simply to stay competitive. Choose the wrong features and the product will be slow to gain market share; more importantly, it will fail to reach its full potential in a market that turns several times a year, affecting revenue.

Extending the life of an existing ASIC is imperative to meet cost goals. The TTM of an ASIC cannot keep pace with the dynamics of this rapidly paced market without revenue loss caused by a missed feature inclusion or design modification. When an ASIC requires a re-spin because of a design error or newly required feature, the market window of opportunity can be missed.



Functionality Supported by Xilinx

Figure 1 – This diagram shows five different blocks marked with a yellow dotted line on two separate boards that can be implemented in a Spartan-3 generation device. Depending on the design requirements and cost target, one or all of the Xilinx-supported blocks on the video/tuner or panel display board could be implemented in a single device.

By incorporating a Xilinx® Spartan™-3 Generation FPGA alongside an ASIC, the life of the ASIC can be increased, allowing the development and engineering costs to be spread out over a larger number of devices. This enables fast TTM and allows many new features to be incorporated at any point throughout the design process.

Coupling the ASIC with an FPGA provides optimum design flexibility, allowing the design to be quickly upgraded and keep pace with the market while also getting the maximum benefits from portions of the design that will be re-used in future products.

For more than five years, Spartan-3 Generation FPGAs have helped designers of digital displays by reducing system cost and complexity while integrating new and unique features. These FPGAs provide the industry's lowest cost solution by eliminating the need for external components.

In this article, I'll explain how Xilinx consumer display solutions incorporate complex video image enhancement algorithms effortlessly, implement hassle-free

commonly used high-speed panel interfaces, and provide instant access to the industry's widest support of I/O interfaces for changing standards and protocols. In addition, they keep your design and IP protected with design-level security technology and support green requirements with dual-power management modes.

Video Image Enhancement

Xilinx Spartan-3 Generation FPGAs provide pre- and post-image processing functions to enhance or extend the life of existing ASICs/ASSPs. As display technology and sizes change, adjustments to the image may be required that the ASIC/ASSP cannot perform. A custom image processing algorithm can also be used for product enhancement and differentiation.

As shown in Figure 1, blocks 1 and 2 can easily implement functions such as motion-adaptive temporal noise reduction, de-interlacing artifact filters, intra-frame noise reduction, color space converters, and dynamic range compression to improve image quality. These functions and more

can be easily implemented with embedded multipliers, DSP blocks, and block RAM to create product differentiation.

Hassle-Free Panel Interfacing

Each new generation of displays integrates a wide variety of panel sizes and types containing distinct interface, timing, and image characteristics. Newer LCD panels incorporate even more complexity, with features such as dynamic backlight and ambient light control. Spartan-3 Generation FPGAs support the latest interface I/O standards, as well as flexible timing controllers to adapt to different panel timing variations.

In addition, you can easily implement image processing to improve the image quality of each panel and enhance features like backlight control for truer colors, deeper blacks, and more detail in dark scenes. This represents some of the functionality that can be accomplished in blocks 2 and 3 (Figure 1).

The best way to keep pace with new panel technology as well as panel interface standards is with the only FPGAs that have



native support (without external components) for the latest differential standards such as Transition Minimized Differential Signaling (TMDS) and Point-to-Point Differential Signaling (PPDS).

Instant Access to Changing Standards and Protocols

Today's displays must support a variety of standards and protocols that range from video input such as DVI and HDMI to internal memory, ASSP/ASIC, and panel interfaces. Spartan-3 Generation FPGAs can help you stay connected with existing interfaces like DDR, DDR2, USB, and Firewire (IEEE1394) standards. Blocks 4 and 5 in Figure 1 show some of the many interfaces/features that may change from model to model.

As consumers demand more features on digital displays, the only way to quickly react is through a programmable solution. Spartan-3 Generation FPGAs offer the ability to support network, hard drive, and multiple memory interfaces as well as the latest digital video interfaces.

The support of different standards or different combinations of standards is as easy as reconfiguration with MultiBoot. MultiBoot allows you to change the functionality by simply reconfiguring the Spartan-3 Generation FPGA, which supports low-cost serial, parallel, and platform flash configuration devices.

Protection with Built-In Design-Level Security

Protecting valuable, proprietary image enhancement algorithms and timing control systems from cloning, overbuilding, and reverse engineering has become increasingly critical. Low-cost, robust security that can be designed quickly to protect

product improvements without impeding quick TTM is a key feature.

Xilinx offers many levels of security that range from hidden bitstreams to advance data manipulation. Spartan-3 Generation FPGAs offer the right security solution to help protect key IP, data, and the complete design in high-volume, low-cost products. With the ease and flexibility to change the security, each model or generation of displays could have a different scheme, making tampering or theft of key circuitry or IP even more difficult.

Go Green

Increased global regulations are requiring more consumer products to reduce standby power consumption. The Spartan-3 Generation offers multiple power-saving modes to help meet your power budget goals. All Spartan-3A, 3AN, and 3A DSP device platforms offer suspend and hibernate modes. The hibernate mode can reduce static power by as much as 99%, while the suspend mode will reduce static power by at least 40%.

Conclusion

Spartan-3 Generation FPGAs offer today's digital display designers the optimal low-cost programmable solution. No other solution combines the flexibility of programmable logic with the native support of cutting-edge I/O and interface support, a wide array of IP, flexible design-level security, and multiple development boards and starter kits to quickly design and test your video applications.

No extra components needed for the built-in security and access to standards that keep you ahead of the game give you the ability to re-use your workhorse ASIC or ASSP and extend its usefulness. ●●●

New Xilinx User Community Works for You 24/7

Launched on August 13, 2007, the Xilinx® User Community (<http://forums.xilinx.com>) is an interactive message board designed for sharing knowledge and information about Xilinx products and technology. Users can start threads, share expertise, exchange ideas, peruse a wealth of valuable information, and submit questions to other users or Xilinx employees.

The community has the following categories, each comprising several boards:

- General discussion
- Silicon devices
- Design tools
- Intellectual property
- Boards and kits

So far, the international Xilinx User Community has more than 1,000 accounts registered, with more than 800 threads posted from around the world.

Don't hesitate. Join the community and start sharing now. Together, let's make the Xilinx User Community an extremely useful resource for all Xilinx users.

Please e-mail forumadmin@xilinx.com if you have any feedback about this community.



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