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X5 210m

PCI Express XMC Module

Features

- Four 250 MSPS 14-bit A/D channels
- +/-1V, 50 ohm, SMA Inputs & Outputs
- Xilinx Virtex5, SX95T
- 512 MB DDR2 DRAM
- 4 MB QDR-II SRAM
- 8 RocketIO Private Links, 2.5 Gbps each
- >1 GB/s, 8-lane PCI Express Host Interface
- Power Management Features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

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Data Sheets
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Perfect for

- Wireless Receiver & Transmitter
- WLAN, WCDMA, WiMAX Front End
- RADAR
- Electronic Warfare
- High Speed Data Recording and Playback
- High Speed Servo Controls
- IP Development

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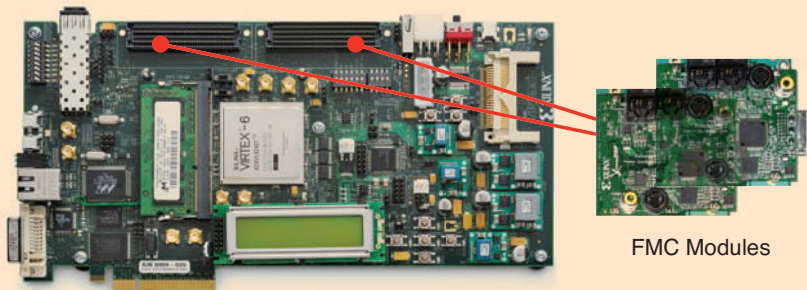
FMC Card Expedites Design Development

One of the key enablers of the Targeted Design Platform approach is the mutual adoption by Xilinx and its network of resellers and IP partners of the FPGA Mezzanine Card from the VITA standards body. The FMC will serve as a standard interface to attach Domain-Specific and Market-Specific Kits from Xilinx and its partners to the Base Evaluation Kits (see figure).

This standards-based approach allows Xilinx and its network of third-party component and board suppliers, including Avnet Electronics, Curtiss-Wright Controls Embedded Computing, Linear Technology and Northwest Logic, to deliver to mutual customers their latest and greatest offerings.

The ANSI-approved VITA 57.1 standard incorporates predefined and fixed locations of parallel and serial I/Os, clocks, JTAG, control signals and power. It uses the well-defined high-performance Samtec SeaRay, supporting Low Pin Count (LPC) 4x40-row and High Pin Count (HPC) 10x40-row connection. For compatibility with older Xilinx FPGA boards, it also includes a voltage-compatible FMC HPC/LPC module.

— Mike Santarini



Spartan-6/Virtex-6 FPGA Base Board

FMC Modules

The FPGA Mezzanine Card (FMC) connection will facilitate rapid IP and kit development.

dynamic power consumption by 10 percent. In addition, the tools have a 28 percent smaller workstation memory footprint than the prior version of ISE.

ISE 11.2 supports the SecureIP simulation model, facilitating compatibility with third-party simulators from Cadence, Mentor Graphics and Synopsys. Also, Mentor Graphics' Precision RTL and Precision RTL Plus products support the Base Targeted Design Platform, as do the Synplify Pro and Synplify Premier tools from Synopsys (Synplicity).

Certainly, another key component of the Base Targeted Design Platform and the overall Targeted Design Platform strategy is IP support. In conjunction with the release of the Base Targeted Design Platform, Xilinx and its IP partners are rolling out numerous soft cores supporting the Spartan-6 and Virtex-6 FPGA families.

The upcoming domain-specific and market-specific offerings will feature some

of these pieces of IP. One, for example, is a PCI Express® DMA Engine from Northwest Logic. Xilinx and Northwest will package the DMA Engine with a demonstration application and drivers to form a complete Connectivity Targeted Reference Design built to support the new Spartan-6 and Virtex-6 devices with the Xilinx base platform.

Xilinx is selling the Spartan-6 FPGA SP601 Evaluation Kit for \$295 and the Virtex-6 FPGA ML605 Evaluation Kit for \$1,995. The Spartan-6 FPGA SP601 Evaluation Kit is available now. The Virtex-6 FPGA ML605 Evaluation Kit will be available in late July.

In the third quarter, Xilinx and reseller Avnet will begin rolling out domain-specific kits for the connectivity, embedded and DSP spaces, followed by market-specific kits for communications, video and broadcast.

For more information, contact your local Xilinx sales office or distributor. ●●