

General Description

The Virtex™-4 QPro™-V family of radiation-hardened FPGAs meet the requirements of space applications that demand high-performance as well as control capabilities. For years, the only solution available to customers with high-performance space applications were ASICs with long development and fabrication times as well as high NREs. Now, Radiation-Hardened Virtex-4 QPro-V FPGAs provide unprecedented integration with Advanced Silicon Modular Block (ASMBL™) architecture, including high-performance logic, PowerPC® embedded processors, XtremeDSP™ signal processing solution and tri-mode Ethernet MACs all in a single device. Radiation-Hardened Virtex-4 QPro-V FPGAs are a powerful alternative to ASIC and antifuse technologies, offering domain-optimized platforms:

- LX – optimized for high-performance logic
- SX – optimized for ultra-high-performance signal processing
- FX – optimized for signal processing

Radiation-Hardened Virtex-4 QPro-V FPGAs are based on commercial Virtex-4 technology, providing enhancements to the popular Virtex and Virtex-II families — making previous-generation designs upwards compatible. Radiation-Hardened Virtex-4 QPro-V FPGAs offer over 350 MHz performance with TID of 250 krad and are manufactured on an UMC 90 nm copper CMOS process technology.

Summary of Radiation-Hardened Virtex-4 QPro-V Family Features

- Full V-Grade manufacturing and process flow
- Guaranteed operation over full military temperature range (–55°C to +125°C)
- Guaranteed 250 krad(Si) total ionizing dose per method 1019
- Guaranteed SEE latch-up Immunity to LET > 100 MeV/mg-cm² per method 1020
- Fully characterized for space radiation effects in heavy ion and proton environments
- SEU mitigation support with TMRTTool software
- Fully tested configuration management IP cores available.
- High reliability ceramic flip-chip packaging technology
- Three Device Architectures: LX/SX/FX
 - ◆ XQR4VLX200:
 - High-density logic applications solution
 - Over 200,000 logic cells
 - ◆ XQR4VSX55:
 - High-performance solution for digital signal processing (DSP) applications
 - ◆ XQR4VFX60/140:
 - High-performance, full-featured solution for embedded processing platform applications
- Xesium clock technology
 - ◆ Digital clock manager (DCM) blocks
 - ◆ Additional phase-matched clock dividers (PMCD)
 - ◆ Differential global clocks
- XtremeDSP slice
 - ◆ 18 x 18, two's complement, signed multiplier
 - ◆ Optional pipeline stages
 - ◆ Built-in accumulator (48-bit) and Adder/subtractor
- Smart RAM memory hierarchy
 - ◆ Distributed RAM
 - ◆ Dual-port 18-Kbit RAM blocks
 - ◆ Optional pipeline stages
 - ◆ Optional programmable FIFO logic automatically remaps RAM signals as FIFO signals
 - ◆ High-speed memory interface supports DDR and DDR-2, SDRAM, QDR-II, and RLDRAM-II.
- SelectIO™ technology
 - ◆ 1.5V to 3.3V I/O operation
 - ◆ Built-in ChipSync™ source-synchronous technology
 - ◆ Digitally controlled impedance (DCI) active termination
 - ◆ Fine-grained I/O banking (configuration in one bank)
- Secure chip AES bitstream encryption
- 90-nm copper CMOS process
- 1.2V core voltage
- IBM PowerPC RISC processor core (FX only)
 - ◆ PowerPC 405 (PPC405) core
 - ◆ Auxiliary processor unit interface (user coprocessor)
- Multiple ethernet MACs (FX only)

Table 1: Virtex-4 QPro-V FPGA Family Members

Device	Configurable Logic Blocks (CLB)					Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	Total I/O Banks	Max User I/O
	Array Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)	XtremeDSP Slices	18-Kb Blocks	Max Block RAM (Kb)						
XQR4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	–	–	13	640
XQR4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	13	576
XQR4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	17	896
XQR4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	–	–	17	960

Radiation-Hardness Assurance

The radiation-hardened Virtex™-4 QPro-V FPGAs are guaranteed for total ionizing dose (TID) life and single-event latch-up (SEL) immunity. Extensive single-event upset (SEU) characterization is performed and reported by the SEE Consortium.

Total Ionizing Dose

Each wafer lot is sampled and tested per Method 1019 to assure that device performance meets or exceeds the guaranteed DC electrical specification requirements, as well as AC and timing parameters at maximum guaranteed total dose levels.

Single-Event Latch-Up

The radiation-hardened Virtex-4 technology incorporates a thin epitaxial layer in the wafer manufacturing process for

latch-up immunity assurance. The qualified mask set is verified in a heavy ion environment under vacuum, and tested at maximum V_{CC} and maximum operating temperature, to a fluence exceeding $1E7$ particles/cm².

Single-Event Upset

Additional experiments are conducted in heavy ion, proton, and neutron environments in order to measure and document the susceptibility and consequence of SEU(s). An industry consortium oversees and validates the test methods, empirical data collected, and resulting analysis.

Conclusions are published on the website as well as international conferences. The Single-Event Effects Consortium Reports can be found at:

<http://parts.jpl.nasa.gov/resources.htm>

Table 2: Radiation Tolerances⁽¹⁾

Symbol	Description	Min	Typical	Max	Units
TID	Total Ionizing dose Method 1019, dose rate ~50.0 rad(Si)/sec	250	–	–	krad(Si)
SEL	Single-event latch-up immunity Heavy ion linear energy transfer (LET)	100	–	–	LET (MeV-cm ² /mg)
SEFI	Single-event functional interrupt GEO 36,000 km typical day	–	1.5E–6	–	Upsets/device/day

System Blocks Common to all Virtex-4 QPro-V Devices

400-MHz Xesium Clock Technology

- Up to twenty digital clock manager (DCM) modules
 - ◆ Precision clock deskew and phase shift
 - ◆ Flexible frequency synthesis
 - ◆ Dual operating modes to ease performance trade-off decisions
 - ◆ Improved maximum input/output frequency
 - ◆ Improved phase shifting resolution
 - ◆ Reduced output jitter
 - ◆ Low-power operation
 - ◆ Enhanced phase detectors
 - ◆ Wide phase shift range
- Companion phase-matched clock divider (PMCD) blocks
- Differential clocking structure for optimized low-jitter clocking and precise duty cycle
- 32 global clock networks
- Regional I/O and local clocks

Flexible Logic Resources

- Up to 40% speed improvement over previous generation devices
- Up to 200,000 logic cells including:
 - ◆ Up to 178,176 internal registers with clock enable (XC4VLX200)
 - ◆ Up to 178,176 look-up tables (LUTs)
 - ◆ Logic expanding multiplexers and I/O registers
- Cascadable variable shift registers or distributed memory capability
- Advanced LUT features (SRL and RAM) can be used in conjunction with configuration scrubbing

400-MHz XtremeDSP Slices

- Dedicated 18-bit x 18-bit multiplier, multiply-accumulator, or multiply-adder blocks
- Optional pipeline stages for enhanced performance
- Optional 48-bit accumulator for multiply accumulate (MACC) operation
- Integrated adder for complex-multiply or multiply-add operation
- Cascadeable multiply or MACC
- Up to 100% speed improvement over previous generation devices.

400-MHz Integrated Block Memory

- Up to 10 Mb of integrated block memory
- Optional pipeline stages for higher performance
- Multi-rate FIFO support logic
 - ◆ Full and empty flag support
 - ◆ Fully programmable almost-full and almost-empty flags
 - ◆ Synchronous/ Asynchronous Operation
- Dual-port architecture
- Independent read and write port width selection (RAM only)
- 18-Kbit blocks (memory and parity/sideband memory support)
- Configurations from 16K x 1 to 512 x 36 (4K x 4 to 512 x 36 for FIFO operation)
- Byte-write capability (connection to PPC405, etc.)
- Dedicated cascade routing to form 32K x 1 memory without using FPGA routing
- Up to 100% speed improvement over previous generation devices.

System Blocks Specific to the Virtex-4 QPro-V FX Family

Dual PowerPC 405 RISC Cores

- Embedded PowerPC 405 (PPC405) core
 - ◆ Up to 350 MHz operation
 - ◆ Five-stage data path pipeline
 - ◆ 16 KB instruction cache
 - ◆ 16 KB data cache
 - ◆ Enhanced instruction and data on-chip memory (OCM) controllers
 - ◆ Additional frequency ratio options between PPC405 and processor local bus
- Auxiliary processor unit (APU) Interface for direct connection from PPC405 to coprocessors in fabric
 - ◆ APU can run at different clock rates
 - ◆ Supports autonomous instructions: no pipeline stalls
 - ◆ 32-bit instruction and 64-bit data

- ◆ 4-cycle cache line transfer

Ethernet Media Access Controller

- IEEE 802.3 compliant
- Operates at 10, 100 and 1,000 Mb/s
- Supports mode auto-detect
- Receive address filter
- Supports multiple PHY (MII, etc.) interfaces through an I/O resource
- Receive and transmit statistics available through separate interfaces
- Separate host and client interfaces
- Support for jumbo frames
- Flexible, user-configurable host interface

Note: RocketIO™ Multi-GigaBit Transceivers (MGTs) are not supported for the Virtex-4 QPro-V FX Family.

Architectural Description: Virtex-4 QPro-V Array Overview

Virtex-4 devices are user-programmable gate arrays with various configurable elements and embedded cores optimized for high-density and high-performance system designs. Virtex-4 devices implement the following functionality:

- I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by programmable I/O blocks (IOBs). The IOBs are enhanced for source-synchronous applications. Source-synchronous optimizations include per-bit deskew, data serializer/deserializer, clock dividers, and dedicated local clocking resources.
- Configurable logic blocks (CLBs), the basic logic elements for Xilinx FPGAs, provide combinatorial and synchronous logic as well as distributed memory and SRL16 shift register capability.
- Block RAM modules provide flexible 18 Kbit true dual-port RAM, that are cascadable to form larger memory blocks. In addition, Virtex-4 block RAMs contain optional programmable FIFO logic for increased device utilization.
- Cascadable embedded XtremeDSP slices with 18-bit x 18-bit dedicated multipliers, integrated adder, and 48-bit accumulator.

- Digital clock manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication/division, and coarse-/fine-grained clock phase shifting.

Additionally, FX devices support the following embedded system functionality:

- Embedded IBM PowerPC 405 RISC CPU (up to 350 MHz) with the auxiliary processor unit interface
- 10/100/1000 Mb/s Ethernet media-access control (EMAC) cores.

The general routing matrix (GRM) provides an array of routing switches between each component. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-4 QPro-V Features

This section briefly describes the features of the Virtex-4 QPro-V family of radiation hardened FPGAs.

Input/Output (SelectIO) Blocks

IOBs are programmable and can be categorized as follows:

- Programmable single-ended or differential (LVDS) operation.
- Input block with an optional single data rate (SDR) or double data rate (DDR) register.
- Output block with an optional SDR or DDR register.
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources.
- Built in data serializer/deserializer

The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:

- LVTTTL
- LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- SSTL 1.8V and 2.5V (Class I and II)

The DCI I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- Hypertransport™ technology
- Differential HSTL 1.5V and 1.8V (Class II)
- Differential SSTL 1.8V and 2.5V (Class II)

Two adjacent pads are used for each differential pair.

Two or four IOB blocks connect to one switch matrix to access the routing resources.

Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a range of

signal delays. This capability is especially useful for synchronizing signal edges in source synchronous interfaces.

General purpose I/O in selected locations (four per bank) are designed to be *regional clock capable I/O* by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

Data serializer/deserializer capability is added to every I/O to support source synchronous interfaces. A serial-to-parallel converter with associated clock divider is included in the input path, and a parallel-to-serial converter in the output path.

An in-depth guide to the Virtex-4 IOB is discussed in [UG070](#), *Virtex-4 User Guide*.

Configurable Logic Blocks (CLBs)

A CLB resource is made up of four slices. Each slice is equivalent and contains:

- Two function generators (F and G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Fast carry look-ahead chain

The function generators, F and G, are configurable as 4-input look-up tables (LUTs). Two slices in a CLB can have their LUTs configured as 16-bit shift registers, or as 16-bit distributed RAM. In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

The Virtex-4 CLBs are further discussed in the *Virtex-4 User Guide*.

Block RAM

The block RAM resources are 18-Kb true dual-port RAM blocks, programmable from 16K x 1 to 512 x 36, in various depth and width configurations. Each port is totally synchronous and independent, offering three read-during-write modes. Block RAM is cascadable to implement large embedded storage blocks.

Additionally, back-end pipeline registers, clock control circuitry, built-in FIFO support, and byte write enable are new features supported in the Virtex-4 FPGA.

The block RAM feature in Virtex-4 devices is further discussed in the *Virtex-4 User Guide*.

XtremeDSP Slices

The XtremeDSP slices contain a dedicated 18 x 18-bit 2's complement signed multiplier, adder logic, and a 48-bit accumulator. Each multiplier or accumulator can be used independently. These blocks are designed to implement extremely efficient and high-speed DSP applications.

The block DSP feature in Virtex-4 devices are further discussed in [UG073](#), *XtremeDSP for Virtex-4 FPGAs User Guide*.

Global Clocking

The DCM and global-clock multiplexer buffers provide a complete solution for designing high-speed clock networks.

Up to twenty DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90°, 180°, and 270° phase-shifted versions of the output clocks. Fine-grained phase shifting offers higher resolution phase adjustment with fraction of the clock period increments. Flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. Virtex-4 devices have 32 global-clock MUX buffers. The clock tree is designed to be differential. Differential clocking helps reduce jitter and duty cycle distortion.

Application Notes and Reference Designs

General application notes and reference designs written specifically for the Virtex-4 family are available on the Xilinx web site at:

http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex4/index.htm.

Aerospace-specific application notes such as configuration scrubbing and SEU mitigation techniques and reference designs for the Virtex-4 QPro-V family of radiation-hardened FPGAs can be found at:

http://www.xilinx.com/products/silicon_solutions/aero_def/index.htm

Virtex-4 QPro-V Family Device/Package Combinations and Maximum I/Os

The Virtex-4 QPro-V family of radiation-hardened FPGAs are available in advanced ceramic flip-chip (CF) column grid technology. This CF packaging technology provides high thermal cycle reliability, passes NASA out-gassing requirements and meets JEDEC Moisture Sensitivity Level 1. The available device and package combinations are shown in [Table 3](#).

Table 3: Virtex-4 Device and Package Combinations and Maximum Available I/Os

Package	CF1140	CF1144	CF1509
Size (mm)	35 x 35	35 x 35	40 x 40
Device	I/O	I/O	I/O
XQR4VSX55	640	–	–
XQR4VFX60	–	576	–
XQR4VFX140	–	–	768
XQR4VLX200	–	–	960

Routing Resources

All components in Virtex-4 devices use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance for high-speed designs.

Boundary-Scan

Boundary-Scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-4 devices, complying with IEEE standards 1149.1 and 1532.

Configuration

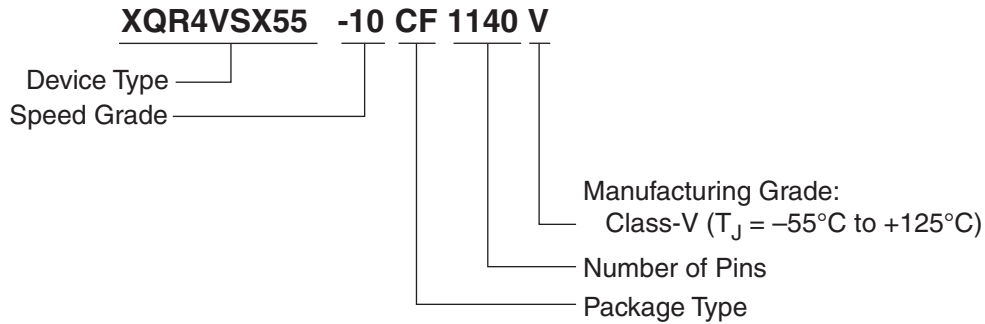
Virtex-4 devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE-1532)

Optional 256-bit AES decryption is supported on-chip (with software bitstream encryption) providing Intellectual Property security.

Virtex-4 QPro-V Ordering Information

Virtex-4 QPRO-V valid ordering combinations are shown in [Figure 1](#). The Virtex-4 QPRO-V family is only available in ceramic flip-chip packages and the -10 speed grade.



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Figure 1: Virtex-4 QPRO-V Ordering Information

Valid Ordering Combinations

XQR4VSX55-10CF1140V	XQR4VFX140-10CF1509V
XQR4VFX60-10CF1144V	XQR4VLX200-10CF1509V

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/04/08	1.0	Initial Xilinx release.
3/31/08	1.1	<ul style="list-style-type: none"> Updated "General Description," page 1. Updated general performance metrics. Updated links.