

Introduction

The LogiCORE™ IP RocketIO™ GTP Wizard automates the task of creating HDL wrappers⁽¹⁾ to configure the high-speed serial GTP transceivers in the Virtex®-5 LXT and SXT platforms. The menu-driven interface allows one or more GTP transceivers to be configured using pre-defined templates for popular industry standards, or from scratch, to support a wide variety of custom protocols. The Wizard produces a wrapper, an example design, and a test bench for rapid integration and verification of the serial interface with your custom function.

Features

- Creates customized HDL wrappers to configure Virtex-5 FPGA RocketIO GTP transceivers
- Users can configure Virtex-5 family GTP transceivers to conform to industry standard protocols using predefined templates, or tailor the templates for custom protocols
- Included protocol templates provide support for the following specifications: Aurora, CPRI™, Fibre Channel 1x, Gigabit Ethernet, HD-SDI, OBSAI, OC3, OC12, OC48, PCI Express® (PCIe®), SATA, SATA II, Serial RapidIO™, and XAUI
- Automatically configures analog settings
- Each custom wrapper includes example design, test bench; and both implementation and simulation scripts

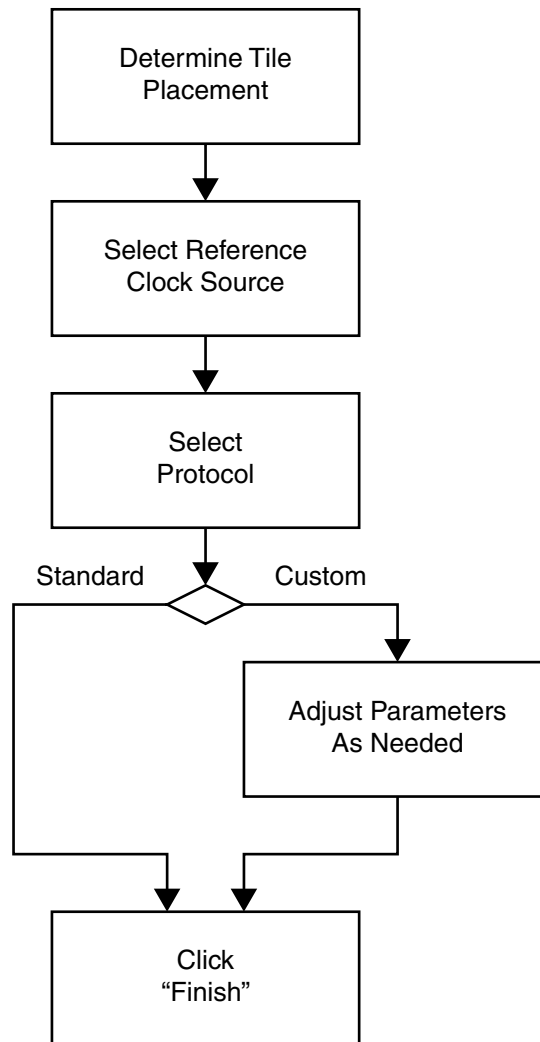
LogiCORE IP Facts	
Core Specifics	
Supported Device Family ⁽¹⁾	Virtex-5 LXT/SXT
Provided with Core	
Documentation	Product Specification Getting Started Guide
Design File Formats	Verilog and VHDL
Constraints File	.ucf (user constraints file)
Verification	Example Design and Test Bench
Instantiation Template	Verilog or VHDL Wrapper
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 10.1 ⁽²⁾
Verification	Mentor Graphics® ModelSim® 6.3c
Simulation	Mentor Graphics ModelSim 6.3c ISE Simulator (ISim) 10.1
Synthesis	Synplicity® Synplify 9.2 XST10.1
Support	
Provided by Xilinx, Inc. at http://www.xilinx.com/support	

1. For more information on the Virtex-5 devices, see [DS100: Virtex-5 Family Overview](#)
2. ISE Service Packs can be downloaded from <http://www.xilinx.com/support/download.htm>

1. See the *Virtex-5 FPGA RocketIO GTP Transceiver Wizard Getting Started Guide* [Ref 1] for an overview of the procedure to create a wrapper.

Functional Overview

Figure 1 outlines the steps required to configure GTP transceivers using the Wizard. Start the CORE Generator™ tool and select the RocketIO GTP Wizard, then follow the steps outlined in the chart to configure the transceivers and generate a wrapper that includes an accompanying example design. If an existing template is being used with no changes, click **Finish**. If modifying a standard template or starting from scratch, proceed through the Wizard and adjust the settings as needed.



DS590_01_01210

Figure 1: GTP Wizard Configuration Steps

See the *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* [Ref 2] for details on the various features and parameters available.

Wrapper Overview

Figure 2 shows the block diagram of the wrapper, example design, and test bench produced by the Wizard.

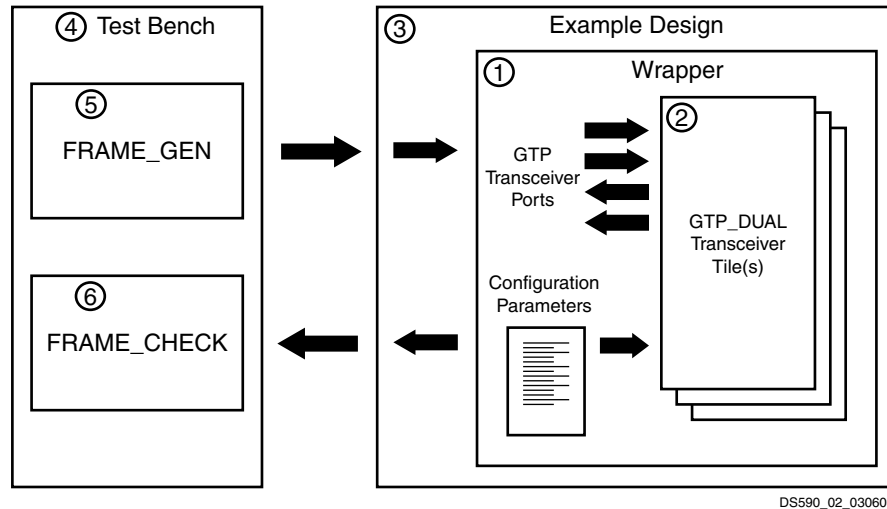


Figure 2: Wrapper Block Diagram

The wrapper comprises six components:

1. **Wrapper:** The specific GTP transceiver configuration parameters set with the Wizard.
2. **GTP_DUAL Transceiver Tile(s):** Instantiated tiles selected with the Wizard.
3. **Example Design:** Temporary top-level design that will be replaced with the actual application.
4. **Test Bench:** Top-level test bench to aid in simulation of the design.
5. **FRAME_GEN Module:** Generates a user-definable data stream for simulation analysis.
6. **FRAME_CHECK Module:** Tests for correct transmission of data stream for simulation analysis.

Reference

1. [UG188](#): *Virtex-5 FPGA RocketIO GTP Transceiver Wizard Getting Started Guide* for a general overview of the wrapper creation procedure.
2. [UG196](#): *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*

Revision History

Date	Version	Revision
03/01/07	1.2	Initial Xilinx release. Wizard v1.4 release.
05/17/07	1.3	Wizard v1.5 release.
08/15/07	1.4	Wizard v1.6 release.
10/10/07	1.5	Wizard v1.7 release.
03/24/08	1.6	Wizard v1.8 release.
03/24/08	1.6.1	Change “test bench” to two words. Add “IP” after “LogiCORE”. Add support link. Move ISE trademark from footnote to table. Add line above copyright statement.
06/26/08	1.9	Synchronize document version with Wizard version. Revise version numbers.
06/27/08	1.9.1	Update release date and trademarks.

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