

Introduction

The JTAGPPC Controller is a wrapper for the JTAGPPC FPGA primitive. The JTAGPPC primitive allows the PowerPC™ to connect to the JTAG chain of the FPGA. For more information about the JTAGPPC primitive, refer to the "PPC405 JTAG Debug Port" section of the [PowerPC 405 Processor Block Reference Guide](#).

Features

- Wrapper for the JTAGPPC primitive
- Enables the debug port of the PowerPC to be connected to the FPGA JTAG chain
- Can connect up to two PowerPC primitives
- Simplified interface to PowerPC processor JTAG port
- Parameter controlled stitching of multi-PowerPC devices

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-II Pro™, Virtex-4™	
Version of Core	jtagppc_cntlr	v2.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	1
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 6.3i or higher	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

JTAGPPC Controller Parameters

The parameters for the JTAGPPC Controller are listed in [Table 1](#).

Table 1: JTAGPPC Controller Parameters

Parameter Name	Description	Allowed Values	Tool Calculated	Type
C_DEVICE	Target device identifier. Used to determine how many PowerPC primitives exist in the part.	2VP4, 2VP7, 2VPX20, 2VP20, 2VP30, 2VP40, 2VP50, 2VP70, 2VPX70, 2VP100, 4VFX12, 4VFX20, 4VFX40, 4VFX60, 4VFX100, 4VFX140	yes	string

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

JTAGPPC Controller I/O Signals

The I/O signals for the JTAGPPC Controller are listed in [Table 2](#).

Table 2: JTAGPPC Controller I/O Signals

Signal Name	Interface	I/O	Initial State	Description
RSTC405RESETSYS ¹	SYSTEM	I		Reset signal from PowerPC 405
TRSTNEG ¹	SYSTEM	I		JTAG Reset signal from user/external logic (Ex: Vision Probe)
HALTNEG ¹	SYSTEM	I		Processor Halt signal from user/external logic (Ex: Vision Probe)
DBGC405DEBUGHALT ⁰ 1	PPC_0	O	HALTNEG	Halt signal to first PowerPC 405
C405JTGTDO ⁰ 2	PPC_0	I		JTAG TDO signal from first PowerPC 405
C405JTGTDOEN ⁰ 2	PPC_0	I		JTAG TDOEN signal from first PowerPC 405
JTGC405TRSTNEG ⁰ 1	PPC_0	O	TRSTNEG	JTAG Reset signal to first PowerPC
JTGC405TCK ⁰ 2	PPC_0	O	same as primitive	JTAG TCK signal to first PowerPC
JTGC405TDI ⁰ 2	PPC_0	O	same as primitive	JTAG TDI signal to first PowerPC
JTGC405TMS ⁰ 2	PPC_0	O	same as primitive	JTAG TMS signal to first PowerPC
HALTNEG ¹ 1	SYSTEM	I		Processor Halt signal from user/external logic (Ex: Vision Probe)
DBGC405DEBUGHALT ¹ 1	PPC_1	O	HALTNEG	Halt signal to second PowerPC 405
C405JTGTDO ¹ 3	PPC_1	I		JTAG TDO signal from second PowerPC 405
C405JTGTDOEN ¹ 3	PPC_1	I		JTAG TDOEN signal from second PowerPC 405
JTGC405TRSTNEG ¹ 1	PPC_1	O	TRSTNEG	JTAG Reset signal to second PowerPC

Table 2: JTAGPPC Controller I/O Signals (Continued)

Signal Name	Interface	I/O	Initial State	Description
JTGC405TCK1 ¹	PPC_1	O	same as primitive	JTAG TCK signal to second PowerPC
JTGC405TDI1 ³	PPC_1	O	same as primitive	JTAG TDI signal to second PowerPC
JTGC405TMS1 ¹	PPC_1	O	same as primitive	JTAG TMS signal to second PowerPC

1.Optional. Leave unconnected if not used

2.Must be connected if core is used

3.Should be left unconnected in single PowerPC devices, required in dual PowerPC devices

Parameter - Port Dependencies

There are no parameter port dependencies.

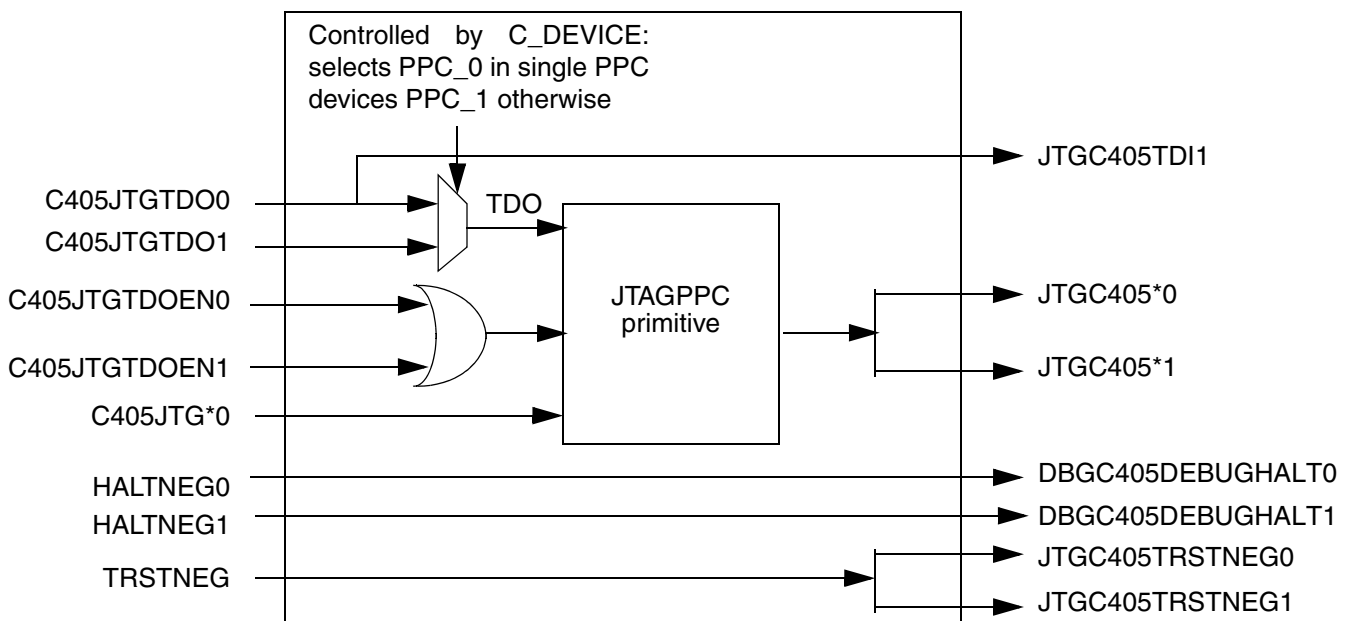
JTAGPPC Controller Register Descriptions

Not applicable.

JTAGPPC Controller Interrupt Descriptions

Not applicable.

JTAGPPC Controller Block Diagram



Design Implementation

Design Tools

The JTAGPPC Controller design is hand written.

XST is the synthesis tool used for synthesizing the **JTAGPPC Controller**. The EDIF netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Target Technology

The intended target technology is an FPGA in one of the following families: Virtex-II Pro, or Virtex-4.

Device Utilization and Performance Benchmarks

The core instantiates the only JTAGPPC primitive on the device. Please refer to the respective FPGA family user's guide for details on JTAGPPC primitive performance.

Specification Exceptions

Not applicable.

Reference Documents

None.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/05/04	1.0	Initial Release.
8/13/04	1.1	Updated for Gmm; reviewed and corrected trademarks usage and supported device family listing.