Zynq UltraScale+ RFSoC
Product Tables and Product Selection Guide

ZYNQ UltraSCALE+

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		Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz				
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB				
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 533MHz				
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core				
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC				
		Static Memory Interfaces	NAND, 2x Quad-SPI				
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet				
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains				
		Security	RSA, AES, and SHA				
		AMS - System Monitor	10-bit, 1MS/s – Temperature and Voltage Monitor				
PS to PL Interface			12 x 32/64/128b AXI Ports				
Programmable Logic (PL)	RF Data Converter Subsystem	12-bit, 4.096GSPS RF-ADC w/DDC	0	8	8	8	0
		12-bit, 2.058GSPS RF-ADC w/DDC	0	0	0	0	16
		14-bit, 6.554GSPS RF-DAC w/DUC	0	8	8	8	16
		SD-FEC	8	0	0	8	0
	Programmable Functionality	System Logic Cells (K)	930	678	930	930	930
		CLB LUTs (K)	425	310	425	425	425
	Memory	Max. Distributed RAM (Mb)	13.0	9.6	13.0	13.0	13.0
		Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0
		UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5
	Integrated IP	DSP Slices	4,272	3,145	4,272	4,272	4,272
		PCI Express® Gen 3x16 / Gen4x8	2	1	2	2	2
		150G Interlaken	1	1	1	1	1
		100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2
		AMS - System Monitor	1	1	1	1	1
	Speed Grades		-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI
Package Footprint	Package Dimensions		PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC
D1156	35x35		214, 72, 208 4, 16, 0, 0				
E1156(1)	35x35			214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	
G1517(1)	40x40			214, 48, 299 4, 8, 8, 8	214, 48, 299 4, 16, 8, 8	214, 48, 299 4, 16, 8, 8	
F1760(1)	42.5x42.5						214, 96, 312 4, 16, 16, 16

1. Available in lidded and lidless stiffener ring packages.

Zynq® UltraScale+™ RFSoCs

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Zynq® UltraScale+™ RFSoC Ordering Information

Footprint

XC	ZU	##	D	R	-1	F	F	V	D	####	E
Xilinx Commercial	Zynq UltraScale+	Value Index	Processor System Identifier D: Quad APU; Dual RPU	Engine Type R: RF Signal	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power	F: Flip-chip w/ 1.0mm Ball Pitch	F: Lid S: Lidless	V: RoHS 6/6 Stiffener	Package Designator	Package Pin Count	Temperature Grade (E, I)

E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

Note: -L2E (Tj = 0°C to +110°C); -L2I (Tj = 0°C to +110°C)

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All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

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