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Addressing the Performance Bottleneck in Modern SoC Design – Serial I/O Connectivity

By: Panch Chandrasekaran

As system-on-chip (SoCs) engineers endeavor to enhance their designs with greater capacity and higher processing speed, the ability to move copious amounts of data in and out of their devices becomes the performance bottleneck. As a result, high-bandwidth serial connectivity is a design requirement in nearly every product.

FPGAs enabled with serial I/O offer the ideal balance of bandwidth, density, performance, flexibility, and cost for SoC designs. Xilinx offers a portfolio of serial I/O technology that addresses the full spectrum of bandwidth requirements for products ranging from commercial video displays to broadcast video ultra-high bandwidth wired telecommunications systems.

Introduction

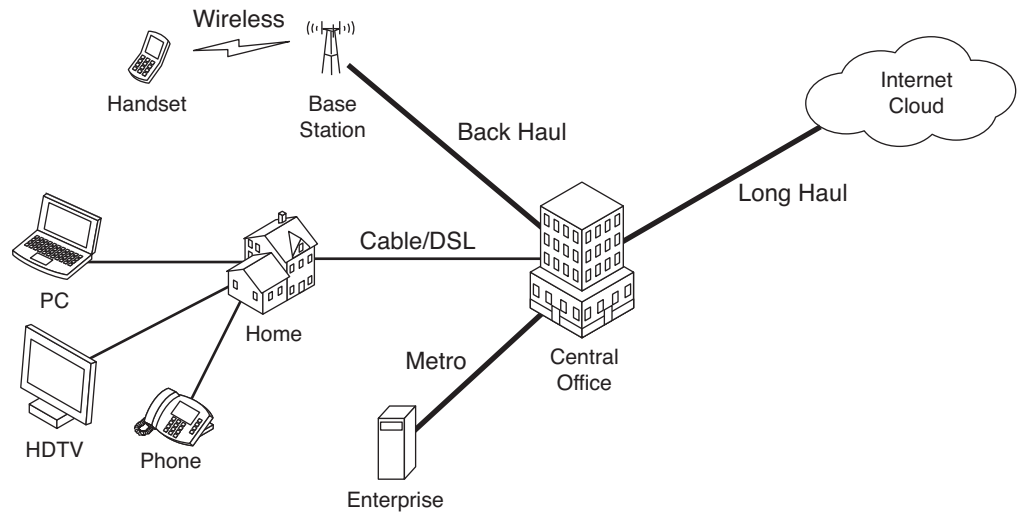
The speed and pervasiveness with which high-speed serial connectivity has risen to the rank of *critical enabling technology* in so many markets should come as no surprise. As the irrepressible global video traffic avalanche overtakes each new market and end-application, it creates an instantaneous increase in bandwidth requirements that makes multi-gigabit serial I/O the best option for SoCs designs.

Xilinx pioneered the evolution of serial I/O solutions in FPGAs. In October of 2002, it announced the *High-Speed Serial Initiative* – a proactive effort to accelerate industry-wide migration to high-speed serial I/O. This new generation of connectivity solutions offered serial-link performance ranging from 3.125 Gb/s to 10 Gb/s and beyond. Since then, five generations of Xilinx® serializer/deserializer (SerDes) transceiver technologies have found their way into a broad continuum of applications and markets stretching from core infrastructure equipment to enterprise systems to home appliances.

Bandwidth Drivers

New devices and services are demanding more bandwidth from the entire spectrum of digital electronic systems (see [Figure 1](#)). Consumer products such as handsets, high-definition TVs, video games, and PCs must now incorporate high-speed serial technology to enable efficient movement and display of massive amounts of video and other data. These devices also act as data sinks that drive bandwidth loads across LAN, WAN, and backbone networks, creating an urgent effort by telecommunication vendors to scale capacity quickly, but cost-effectively. Witness the wireless service providers that have already begun expanding their 3G networks and rolling out 4G networks to enable delivery of even more content to mobile handsets and PCs.

Bandwidth requirements in the enterprise market are also rapidly increasing. More companies are adopting telepresence and high-definition video conferencing technologies to control travel costs. The growing momentum for web-delivered and supported Software-as-a-Service (SaaS) and the ongoing battle to consolidate data centers (with increased capacity) are major bandwidth drivers that necessitate faster serial I/O links. Similarly, the adoption of high-speed serial I/O technology in the aerospace, defense, medical instrumentation, and automotive infotainment markets has also been accelerated by the demands for greater speed and resolution in digital imaging and video technologies.



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Figure 1: Accelerating Bandwidth Requirements in Enterprise Markets

Serial Connectivity Application Landscape

The global landscape for solutions in the serial connectivity domain can generally be divided into three performance categories: mainstream, high-end, and ultra-high-end. The system designers working in these categories have different levels of expertise in serial I/O design, different problems to solve, and different design goals.

Mainstream designers build high-volume products for the consumer electronics, industrial instrumentation, and communication markets, where cost and time to market are of paramount importance. Although familiar with traditional parallel I/O design requirements, mainstream designers must now use multi-gigabit serial I/O links in their systems, and are therefore far less familiar with the analog design challenges that await. These designers need comprehensive, easy-to-use design platforms that simplify the serial I/O design effort, allowing them to spend the majority of their time and effort adding differentiated value to their products. See [Table 1](#).

Table 1: Serial Connectivity Categories

	Mainstream	High-End	Ultra High-End
Line Rates	Up to 3.2 Gb/s	Up to 6.5 Gb/s	Beyond 11 Gb/s
Focus	Simplicity, ease of design, and results	Increased capabilities and performance	Achieving breakthrough bandwidth
Typical FPGA family	Spartan LXT FPGAs	Virtex LXT FPGAs	Virtex HXT FPGAs
Market Segments			
Wired	Low-cost, efficient protocol bridging	Advanced protocol mapping, performance optimized backplanes	Cutting edge protocol support, advanced processing capabilities
Wireless	Low-cost, Femto/Picocell deployment	Cost/power efficient, mainstream deployment	
Video Broadcast	Efficient processing and routing capabilities	Accelerated encoding and processing	High-data aggregation/routing, advanced processing capabilities
Consumer	Cost-effective integration, simplified serial interfaces		
Automotive	Low-power, cost-optimized, and flexible serial I/O connectivity		

High-end designers need to pack more performance and bandwidth into the smallest possible footprint, so power density is a key consideration. Also, as serial link speeds increase, signal integrity becomes more difficult to achieve and maintain and is therefore a critical factor in every design. These designers are more familiar with serial I/O design than mainstream engineers, having spent the last five to ten years battling the signal integrity wars in their own domain. Thus, given a familiar design environment with the right IP library, reference designs, and development boards, mainstream designers can expend the majority of their effort overcoming performance bottlenecks.

Ultra-high-end designers have worked the longest with serial I/O and have one fundamental objective—to keep pushing the performance envelope. These designers must fit several multiples of 10G ports into the previous design's footprint without overwhelming the system. Although performance is preeminent, flexibility is also important to the ultra-high-end designer since standards in this domain are rarely stable. Even with stable standards, the ultra-high-end designer needs a design environment that permits probing and tweaking every corner of the design to gain and keep an edge on competitors.

Xilinx High-Speed Serial I/O Solutions

Addressing the serial I/O needs of these designer profiles begins with providing the right silicon—an FPGA that delivers the optimum price, performance, power density, and transceiver capabilities. However, a truly effective design platform must offer a holistic, well integrated complement of design resources that extends well beyond the silicon—all designed to aid in the creation of reliable, system-level, high-speed serial links that are suitable for a specific application or market.

These design resources include:

- Silicon platform (FPGA)
- Transceivers
- Boards
- IP
- Reference designs
- Kits
- Design and debugging tools
- Design support
- Education
- Engineering services

Starting with Silicon

Xilinx created the Virtex®-6 and Spartan®-6 FPGA families to serve as the foundation for comprehensive design platforms that target: wired communications; wireless communications; video broadcast; aerospace; defense; industrial; scientific; medical; automotive infotainment; and consumer markets (see [Table 1](#)). These disparate markets share a common set of serial connectivity requirements and design challenges, all of which Xilinx FPGAs address.

The end products in each of these target markets need serial transceivers to implement industry-standard protocols for moving data between boxes, boards, and/or devices. They also need a high-performance logic fabric to instantiate the communications protocol, bridge between different protocols, and provide other application-specific functions. With the amount of data these products must process and deliver, designers also require high-speed, parallel I/O for building high-bandwidth, data-buffering memory subsystems, using commodity memory devices as well as a CPU to perform system control and data processing functions. The Virtex-6 and Spartan-6 FPGA families fit the bill.

Virtex-6 FPGAs

The Virtex-6 FPGA family comprises three sub-families that deliver different feature mixes to address a diversity of end-product design requirements:

- Virtex-6 LXT FPGAs serve applications that require high-performance logic, DSP, and serial connectivity, with up to 36 low-power GTX 6.5 Gb/s serial transceivers.
- Virtex-6 SXT FPGAs target applications that require ultra high-performance DSP and serial connectivity, with up to 36 low-power GTX 6.5 Gb/s serial transceivers.
- Virtex-6 HXT FPGAs are optimized for communication, switching, and imaging systems that require the highest-speed serial connectivity, with up to 24 GTH 11.18 Gb/s serial transceivers and 48 GTX 6.5 Gb/s serial transceivers.

The combination of advanced silicon technology, innovative circuit design techniques, and architectural enhancements enables all Virtex-6 FPGAs to deliver significantly lower power consumption, higher performance, and lower cost than previous-generation Virtex devices and competing FPGA offerings. Built on a 40 nm process, the Virtex-6 FPGA family provides 15% higher performance and 15% lower power consumption than competitive 40 nm FPGA offerings. To this, Xilinx has added features such as second-generation integrated blocks for PCI Express and third-generation Tri-mode Ethernet MAC blocks to easily implement popular

interfaces, flexible block RAM for on-chip data buffering, and built-in DSP acceleration engines. To support the high-bandwidth data buffering using external memory subsystems, SelectIO™ technology provides built-in support for DDR3 SDRAM.

Spartan-6 FPGAs

Spartan-6 LXT FPGAs are the first to provide the necessary logic capacity, performance, power consumption, and price points to enable mainstream designers to use FPGA-based serial technology for end-system deployment in the consumer and automotive infotainment markets. Fabricated on a low-power 45 nm, 9-metal-layer, dual-oxide process technology, these FPGAs include up to eight 3.125 Gb/s GTP transceivers and an integrated Gen 1 endpoint function for PCI Express® (both derived from proven Virtex FPGA family technology) to simplify connectivity to processors. Integrated memory controller blocks simplify interfaces to DDR3-800 memory for high-bandwidth data buffering.

Optimized Transceiver Technology

Together, the Virtex-6 and Spartan-6 families fulfill all of the requirements across all three of the aforementioned serial connectivity categories: mainstream, high end, and ultra high end. To address the broad range of serial I/O requirements (in terms of bandwidth, cost, and complexity) represented by the target markets in each category, Xilinx offers a portfolio of transceivers, each optimized for a specific range of performance and price.

GTP - The Mainstream Transceiver

The connectivity requirements of mainstream applications are satisfied by protocols that run at speeds below 3.125 Gb/s, such as PCI Express 1.0, Gigabit Ethernet, XAUI, Serial RapidIO (SRIO), SATA, DisplayPort, V-by-One, and triple-rate SDI.

Achieving the necessary signal integrity for this category is less challenging than for the other two, however, transceivers for mainstream products must also provide low cost and low power.

The Xilinx low-power GTP transceiver, initially released in the Virtex-5 LXT FPGA, provides 614 Mb/s to 3.125 Gp/s connectivity in the low-cost Spartan-6 LXT FPGA. This transceiver offers numerous features specifically designed to aid the designer:

- GTP transmitters implement the physical media attachment (PMA), part of the physical layer that performs analog-digital functions, with programmable output levels to compensate for external signal attenuation.
- Programmable pre-emphasis compensates for unavoidable external low-pass attenuation.
- Receiver PMA circuitry includes linear equalization to compensate for external low-pass attenuation and to keep the eye open, whether building chip-to-chip connections or establishing channels across a backplane.
- Implementation of the physical coding sub-layer (PCS), part of the physical layer that controls logic functions, includes built-in 8B/10B encoding/decoding for protocols such as Gigabit Ethernet.

GTX - The High-End Transceiver

The bandwidth requirements in high-end applications call for 6 Gb/s class transceivers to support higher speed variants of mainstream protocols, such as

PCI Express 2.0, SRIO, RXAUI, and Interlaken. At these speeds, signal integrity challenges increase significantly, driving a requirement for additional, more sophisticated, signal conditioning techniques. The 6.5 Gb/s GTX transceivers, first available on Virtex-5 FXT FPGAs, provide 150 Mb/s – 6.5 Gp/s connectivity on all members but one of the Virtex-6 families.

For best results in driving challenging links, GTX transmitters include pre-emphasis and post-emphasis capabilities with programmable drive strengths. Because signal attenuation becomes a bigger issue at higher speeds, GTX receivers incorporate two types of receive equalization circuitry to help open the signal eye-linear equalization and decision feedback equalization (DFE). GTX transmitter and receiver circuits each incorporate gearboxes for efficient 64B/66B and 64B/67B encoding and decoding, respectively. Built-in pattern generators and pattern checkers further simplify implementation of industry-standard protocols.

GTH - The Ultra-High-End Transceiver

The drive for 40G and 100G networks creates a requirement for transceivers supporting line rates of 10 Gb/s or more. Protocols in the 10 Gb/s range have extremely stringent jitter requirements. The GTH transceivers available on Virtex-6 HXT FPGAs support line rates from 9.95 Gb/s to beyond 11 Gb/s and incorporate phase-locked loop (PLL) circuits optimized for low jitter at these speeds. This approach avoids the compromises inherent in other transceivers that attempt to cover the range for 2.488 Mb/s to 11 Gb/s and beyond with a single PLL design. The GTH transceiver incorporates equalization circuits such as transmit pre-emphasis, Rx linear equalization, and DFE. An adaptive equalization engine utilizes the internal eye-scan circuitry and automatically tunes the equalization settings for the highest link performance. The GTH transceiver also integrates the 64B/66B coding scheme required for the key protocols in the 10 Gb/s speed range.

IP

Across the serial spectrum, there are numerous serial protocols that cater to the specific needs of application requirements in the aforementioned target markets with line rates ranging from only a few hundred Mb/s to greater than 11 Gb/s. Xilinx and its ecosystem partners (which includes hundreds of IP design houses) provide a comprehensive serial connectivity IP portfolio that contains over 300 of the most popular design blocks, such as PCIe, Interlaken, and OTU blocks.

Targeted Reference Designs

The best way to help architects and designers optimize their time is to enable them to spend the majority of it creating the key value-added features that differentiate their products. The Connectivity Domain kits for Virtex-6 and Spartan-6 FPGAs provide targeted reference designs that integrate the most common building blocks and integrated blocks, such as memory controllers and PCIe/EMAC blocks, needed for that domain. The advantage of this modular design approach is that system designers can begin their design implementations with these reference designs and customize them at will.

For example, the Virtex-6 LXT FPGA PCIe-to-XAUI Targeted Reference Design follows this modular concept to include key building blocks, such as an integrated block for PCIe, GTX transceivers, the Xilinx XAUI IP LogiCORE™ solution and other IP deliverables from Xilinx Alliance Partners. Xilinx also provides software device

drivers and an example application with source files, which the customer's software group can modify to target any underlying hardware changes required in the design.

Kits

Xilinx creates three types of kits that correspond to the three foundational layers of a Xilinx Targeted Design Platform: the evaluation kit, the domain-specific (or Connectivity) kit, and the market-specific kit. Evaluation kits provide all of the necessary platform components required to begin working with a new device. Domain-specific kits target one of three fundamental designer personas: the embedded designer, the DSP designer, and the connectivity designer. Market-specific kits target particular markets and/or applications.

The Virtex-6 FPGA ML605 Evaluation Kit provides a development environment for system designs that demand high-performance serial connectivity and advanced memory interfacing. The ML605 is supported by pre-verified reference designs and provides industry-standard FPGA Mezzanine Card (FMC) connectors to decouple I/O and other functional elements from the FPGA to enable scaling and customization without requiring changes to the ML605 base board. Integrated tools help streamline the creation of elegant solutions to complex design requirements.

The Spartan-6 FPGA SP605 Evaluation Kit delivers all the basic components of the Xilinx Base Targeted Design Platform for developing broadcast, wireless communications, automotive, and other cost- and power-sensitive applications that require transceiver capabilities in one package. The kit provides a flexible environment for higher level system design, including applications that need features such as high-speed serial transceivers, PCI Express, DVI, and/or DDR3. It also includes FMC connectors for scaling and customization to address specific applications and markets. Along with the development board, cables, and documentation, this kit integrates the hardware, software, IP, and pre-verified reference designs so the designer can begin development right out of the box.

ML605 and SP605 evaluation kits act as the base for Connectivity Domain Kits that enable designers to extend the functionality of the base boards to perform advanced functions and implement designs to address high-speed serial interfaces, such as XAUI, GbE, PCI Express 2.0, etc.

In addition to the Connectivity Domain Kits, market-specific boards and kits (some based on the ML605 and SP605 boards) can assist designers with the start of their designs. See [Figure 2](#).



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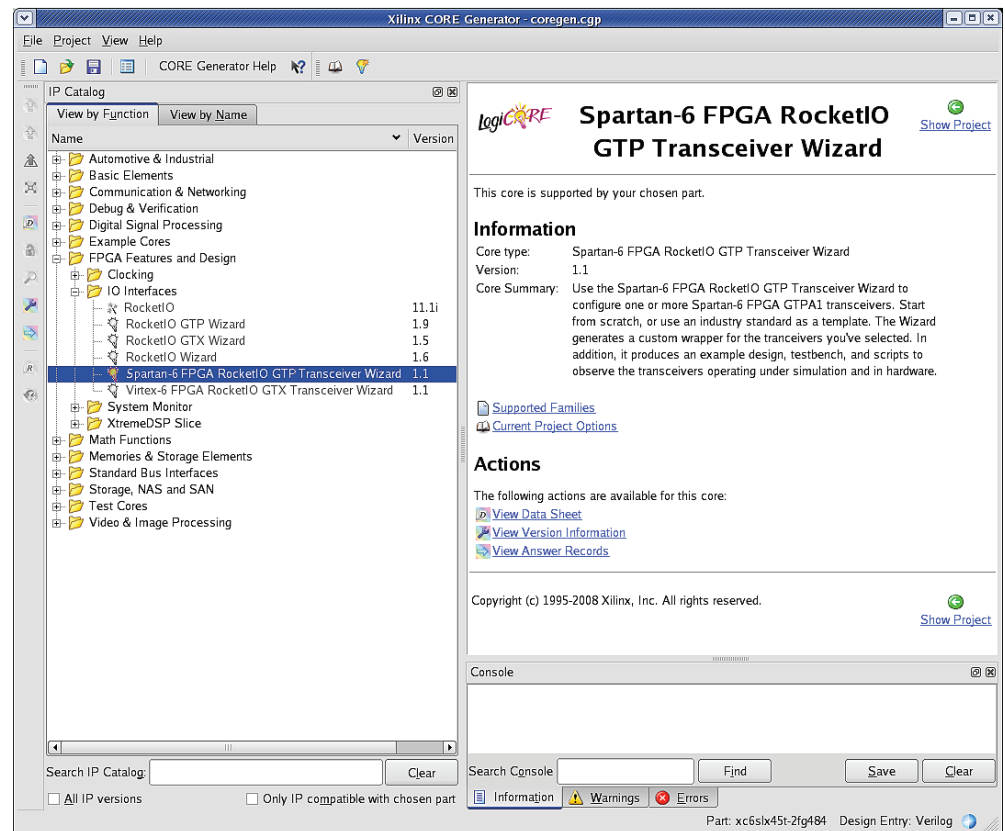
Figure 2: Spartan-6 FPGA Evaluation Kit

Serial I/O Design and Debugging Tools

Ten years ago, if designing high-speed serial I/O into a system, a designer was probably an analog-savvy backplane engineer in the telecom space using discrete serializers that were, at best, difficult to work with, if not downright temperamental. Since then, external chip solutions have emerged that are significantly easier to use and much more stable, offer much higher performance, and exhibit remarkable flexibility. This serial I/O evolution has paved the way for digital designers that have little or no knowledge of the seemingly esoteric world of signal integrity to keep pace with their market's burgeoning bandwidth requirements. Today, supporting this range of designer experience requires design and debugging tools that offer both simplicity and sophistication.

Wizards

Xilinx provides configuration wizards (see [Figure 3](#)) for the GTP, GTX, and GTH transceivers that simultaneously serve the ease-of-use needs of the truly novice mainstream designer and the design performance and flexibility requirements of the signal integrity expert. The former merely selects a location on the FPGA to place the tile and a reference clock source, chooses the desired protocol (e.g., 10GE) from a drop-down menu, and with the push of a button, the configuration wizard creates an RTL wrapper and transceiver that is the default implementation of that protocol's transceiver design, which the designer can then instantiate in the FPGA design.



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Figure 3: Configuration Wizards Create a Standard Serial I/O Transceiver

The ultra-high-end designer can start with the default setting but will typically begin customizing the design through the myriad of switches in the configuration wizard, either to accommodate changes in the standard or the custom requirements of the design.

Internal Bit-Error Rate Tester (IBERT)

One of the most critical stages of a product is the system bring-up. Engineers test/debug the system and make the necessary adjustments to the "knobs" that are available. This can be a time consuming process that requires expensive lab equipment that can cost the designer well over \$50,000.

The ChipScope™ Pro analyzer is a Xilinx debug tool that lets the designer see into a logic design, isolate and diagnose a problem, and change settings to fix it. IBERT is an add-on to the ChipScope Pro tool that was created for transceiver debug. It allows the designer to adjust all of the parameters of the transceiver, including some more advanced settings like termination resistors that are accessible only through the FPGA's Dynamic Reconfiguration Port (DRP).

The designer can also use IBERT to access the bit-error-rate tester hard-coded into every transceiver to:

- Send a PRBS across the channel to help debug
- Change streams for different data patterns
- Check the status (e.g., is the link locked up/working)?
- Exercise individual control for multiple transceivers
- Perform near-end and far-end loopback to isolate and debug the link
- Monitor the bit error rate in the IBERT window
- Change the signal voltage swing level
- Change the amount of pre-emphasis
- Change the receive equalization
- Change the DFE

IBERT allows the designer to get familiar with all of the transceiver options/switches, generate traffic streams, and change parameters at will. Among the more advanced features offered by IBERT is the automated eye-scan capability for finding the best transmit and receive settings. Eye scan is a graphical margin analysis technique that uses eye mapping to aid in the design of high-speed SERDES channels with predictable, reliable results and maximum design margins. Eye scan sweeps multiple parameters of the receiver, plotting bit error rate versus deflection from ideal settings. Eye scan can determine in seconds both the achievable bit error rate and margin, while helping the designer explore the effect various parameter changes have on the design—something that would otherwise take weeks to accomplish.

Transceiver Simulation Models

Simulation is an essential but time-consuming part of transceiver design. The historic use of HSPICE (analog) models were useful when designs rarely required more than two transceivers, and each transceiver had one driver and one receiver. Adding transmit pre-emphasis, receive equalization, and DFE (especially difficult to simulate this digital function with analog models) causes transistor counts and simulation time to increase greatly.

Today, designers are working with multiple transceivers and must employ every possible technique to ensure stable and reliable signal integrity. This has given rise to the adoption of algorithmic (or behavioral) models for complex serial designs. Xilinx algorithmic models run much faster than HSPICE models. They simulate digital functionality more easily and enable the designer to instantiate and simulate multiple transceivers at the same time.

System-Level Signal Integrity

Experienced serial I/O designers recognize the importance of treating signal integrity as a system-level issue when designing multi-gigabit serial links. At these speeds, bit periods are so small that any added noise on the signal affects the timing and noise margins. To put this into perspective, the effect of a 20 ps jitter is virtually negligible on a 1 Gb/s signal, but it represents about 20% of the bit period in a 10 Gb/s signal—sufficient to drive bit-error rates past acceptable limits. Moreover, as speeds increase, small-geometry physical structures in the serial link, such as vias and connectors, start playing a pivotal role in achieving acceptable signal integrity.

Thus, for high-speed serial connectivity solutions, the term signal integrity applies to the quality of the signal across the entire continuum, from the silicon through the package to the board to the backplane. Consequently, system-level signal integrity can be viewed as having three distinct categories:

- Silicon-level signal integrity
- Package-level signal integrity
- Board-level signal integrity

Silicon-Level Signal Integrity

Choosing the right device, one with transceivers that produce the cleanest possible signal and offer the most robust capability for accurately reading the received signal, simplifies system-level and board-level design. Xilinx serial transceivers incorporate a variety of equalization circuits to ensure that the receiver sees an open eye. The line rate determines the choice of technique. Transmitters on all Virtex-6 and Spartan-6 FPGAs provide transmit pre/post-emphasis to compensate for high-frequency signal attenuation. To deal with the signal integrity challenges of 6.5 Gp/s links, GTX transceivers add linear equalization and DFE circuits to the receiver PMA.

GTX and GTH transceivers both employ PLL circuitry, optimized for the lowest possible jitter within their respective speed ranges. The result is greater margin for link performance.

Architectural Considerations

Spartan-6 LXT and Virtex-6 LXT and SXT FPGAs incorporate a highly flexible clocking architecture. For example, a GTX transceiver in Virtex-6 FPGAs provides independent PLLs for each transmit (TX) and receive (RX) channel within the transceiver. The resulting independent clock domains provide tremendous flexibility to maximize the effective number of channels supportable in a given design. For applications where the TX and RX datapaths operate in the same line rate range, the RX PLL can be shared between the TX and RX datapaths and the TX PLL can be powered down to conserve power.

For the high-end GTH transceiver, Xilinx incorporates an LC-tank-based voltage controlled oscillator (VCO) to obtain excellent phase noise performance, a feature critical to the designer attempting to meet and exceed the stringent jitter requirements of protocols such as SFP+ (small form factor pluggable transceivers), OC-192 (standard for a network line with transmission speeds of up to 9953.28 Mb/s), and 10G-BASE KR (the latest IEEE Std 802.3ap v3.3 for the operation of 10 Gb/s Backplane Ethernet (10GbE)).

Rather than clock multiple channels of transceivers with a single PLL, the GTH transceiver utilizes a quad architecture where a single PLL clocks four channels. This provides the flexibility to incorporate multiple independent clock domains required for multi-protocol applications.

The quad architecture also plays an important role in achieving acceptable signal integrity. An FPGA is an extremely noisy environment, and high-speed signals (especially those at or above 10 Gb/s) are susceptible to noise coupling as the FPGA logic gets filled and the number of active serial and parallel I/Os increase. The longer the high-speed signals have to travel, the more susceptible they become to noise coupling. The GTH transceiver's quad-based architecture confines the multi-gigabit signals to within a quad, thereby isolating it from noise sources.

Equalization

As signals travel across the printed circuit board (PCB), the high-speed components of a signal get attenuated, thereby negatively impacting the bit error rate of the link. As speeds increase, this attenuation becomes increasingly problematic. Although effective at speeds below 5 Gb/s, linear EQ techniques alone are insufficient at higher frequencies. Designing at these speeds requires additional techniques such as DFE. At greater than 10 Gb/s, signal equalization becomes critical for anything more than a simple chip-to-chip connection. See [Table 2](#).

Table 2: GTP, GTX, and GTH Transceivers Equalization Circuits

Transceiver	Tx Pre-Emphasis	Rx DFE	Rx Linear EQ
Spartan-6 FPGA GTP	Yes	No	Yes
Virtex-6 FPGA GTX	Yes	Yes	Yes
Virtex-6 FPGA GTH	Yes	Yes	Yes

Package-Level Signal Integrity

The effect packaging can have on signal integrity in high-speed serial I/O design is often overlooked and usually underestimated. Xilinx has incorporated a third-generation of high-performance packaging designed specifically to address high-speed signaling needs. See [Figure 4](#).

Key features of this packaging design include:

- Solid power planes within the package
- On-package decoupling caps for noise filtering, minimizing onboard components
- A unique pinout that provides the most optimal return paths for high-speed signals
- Isolation of parallel and serial I/O to minimize noise coupling and maximize IO performance and usage

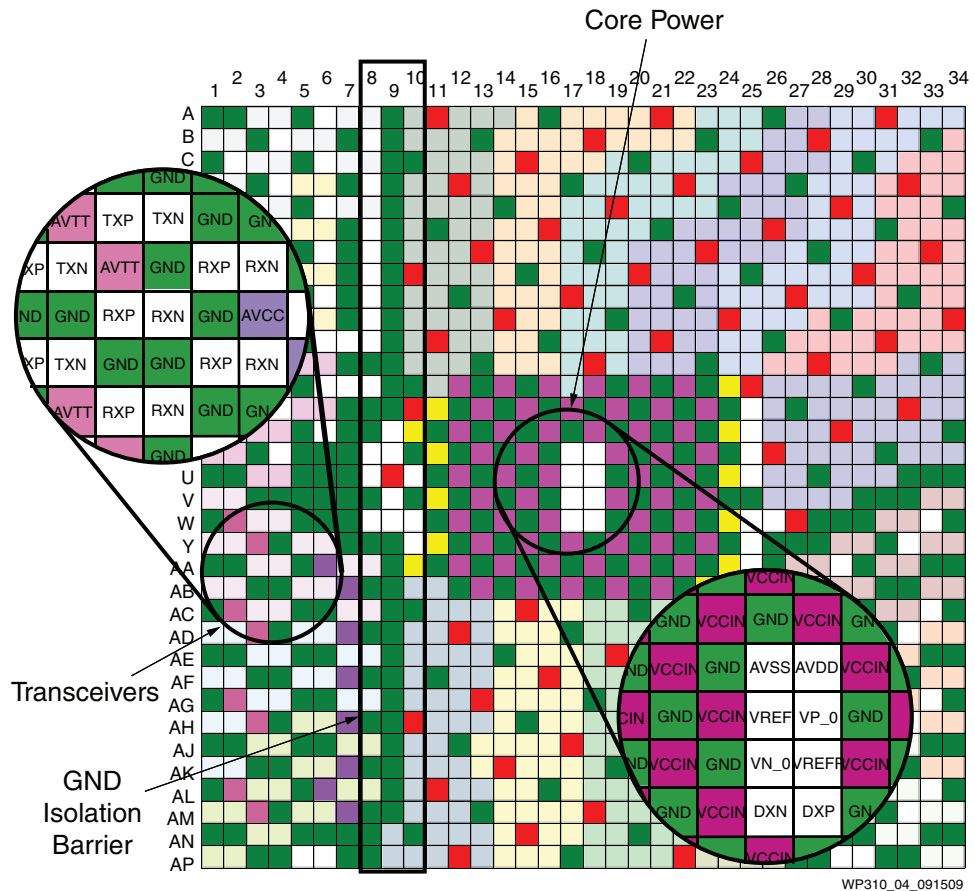


Figure 4: Virtex-6 FPGA Package Optimized for Signal Integrity

The results achievable with this packaging technology are nothing short of astounding-30dB isolation between channels and over 40dB isolation between TX and RX.

Board-Level Signal Integrity

After seven years of research and development that has produced five generations of transceivers, it is an understatement to say that Xilinx has invested heavily in the research of board-level aspects of signal integrity. Throughout that research, the three areas that impact board-level signal integrity the most are: board layout, the power distribution network, and clocking.

Layout

As previously mentioned, physical structures become more visible to the signal at higher speeds. Geometries of just a few millimeters can severely alter the signal characteristics. In an effort to provide the most complete and most robust platform possible, Xilinx builds backplanes and test boards with different structures, connectors, vias, and PCB materials to study their impact on the signals. Having performed extensive analyses on these layout components, Xilinx is better equipped to provide high-speed boards and layout guidelines to its customers, eliminating the need for customers to conduct these exhaustive analyses themselves. See [Figure 5](#).

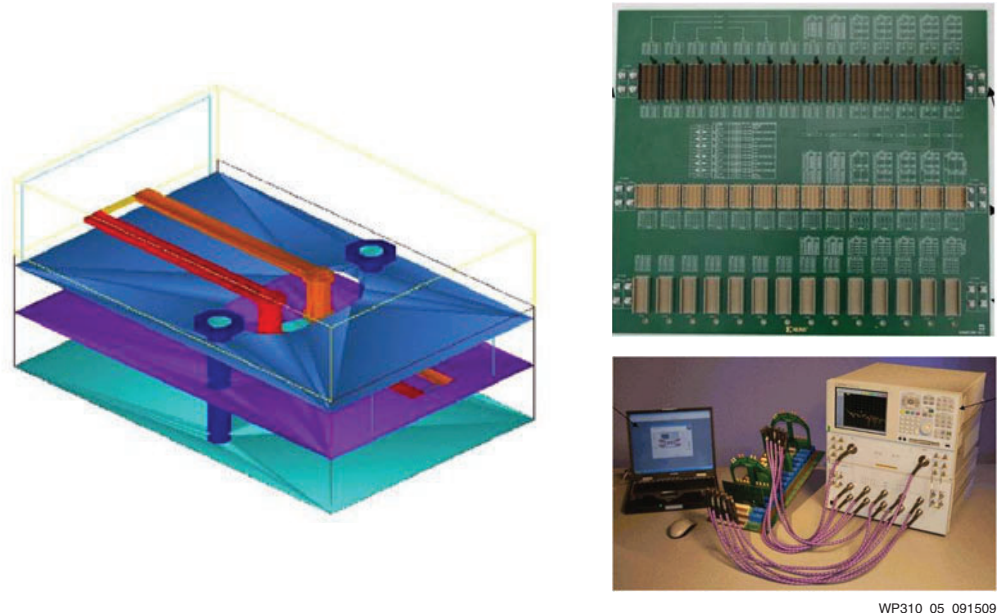


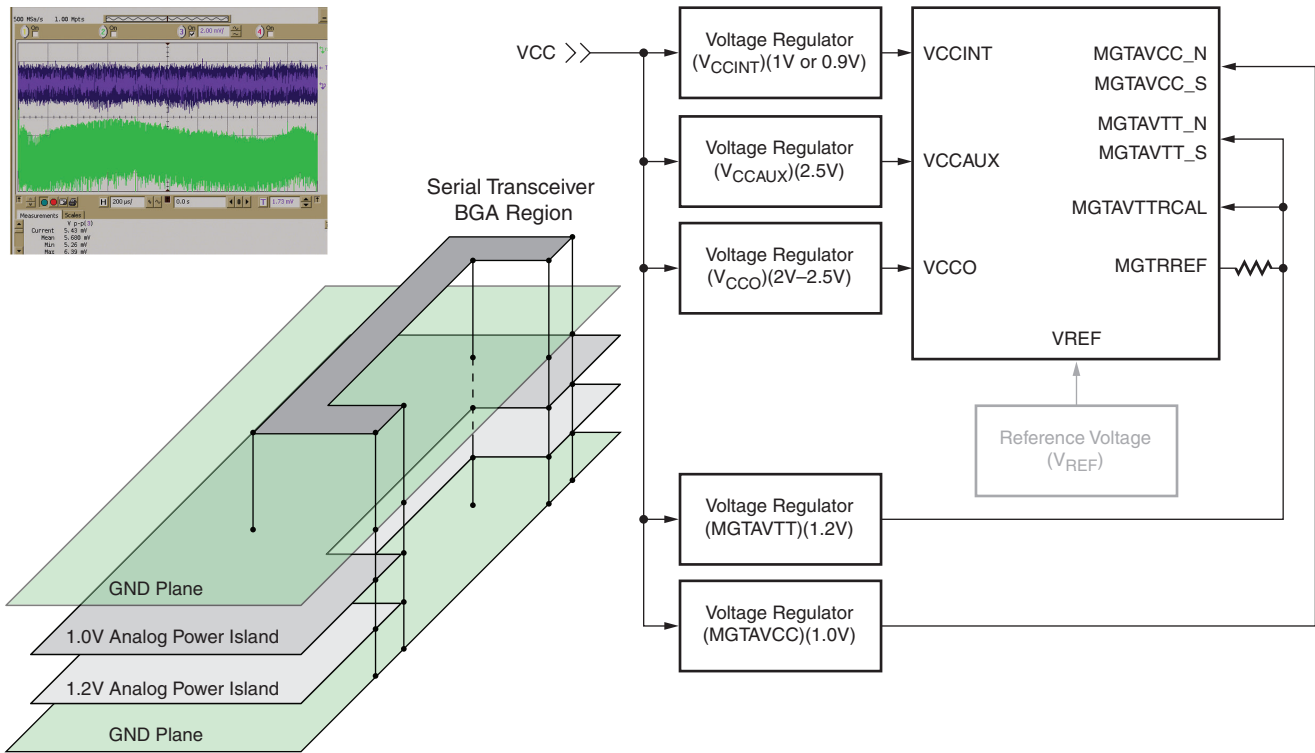
Figure 5: Critical Layout Guidelines Provided by Xilinx

Power Distribution Network

A clean power supply is essential to maintaining good jitter performance. Noise in the power supply translates directly into poor jitter performance both at the transmitter and the receiver. This also creates problems for the board design, area and efficiency. Historically, transceiver vendors have used linear regulators (clean, but very inefficient) to clean up the supply noise. This necessitates the use of several regulators to meet their power requirements. Moreover, many FPGAs force designers to use a number of onboard capacitors and beads to filter out the noise.

Xilinx has approached power distribution from a holistic point of view with solutions that start at the silicon and extend out to the board, all with a focus on simplicity and performance:

- The number of supply rails required by the transceivers in Virtex-6 and Spartan-6 devices is reduced to 2 for GTP and GTX transceivers, and 3 for GTH transceivers.
- Integration of capacitors at the die and in the package filter out noise right at the source, greatly reducing the component count on the board.
- Xilinx has worked with industry-leading power supply vendors to provide switching regulators that significantly ease the cost and burden of customer power supply designs.
- Xilinx provides comprehensive layout guidelines in combination with the switching regulators to achieve the level of performance that in the past would require many times more onboard components.



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Figure 6: Simplifying Board Design via Power Distribution Network Analysis

Clocking

All transceiver PLLs synthesize a high-speed clock using a lower speed reference clock. Thus, the quality of the reference clock has a strong influence on both the jitter generation of the transmitter and the jitter tolerance at the receiver.

Specifying the reference clock requirements to account for the jitter characteristics across the required frequency domain has historically been a challenge for transceiver vendors. Although the cleanest reference clocks provide the cleanest jitter performance, they can also prove too expensive. To help designers choose the right reference clocks for their particular design, Xilinx applications teams have invested considerably in the analysis of clock requirements and solutions across a wide spectrum of markets and applications.

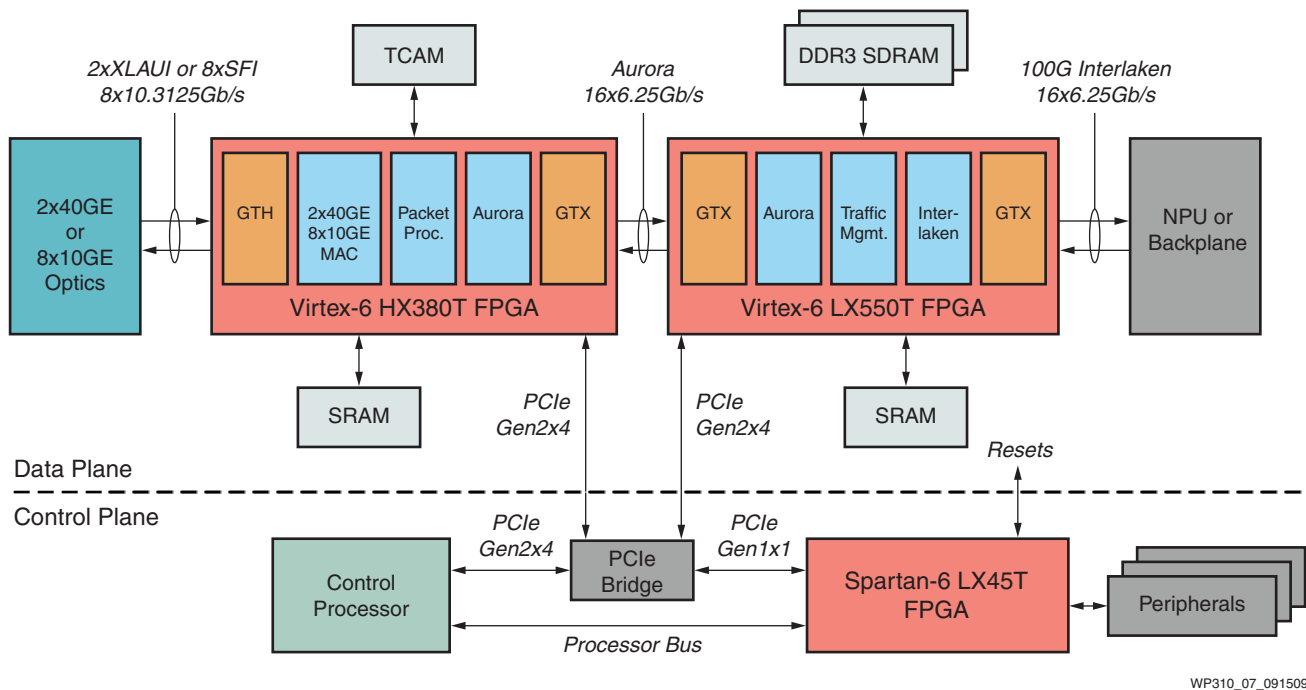
As part of this effort, Xilinx has partnered with clock vendors like SiLabs, IDT, and Vectron to provide the right reference clock solutions for a variety of protocols. Xilinx also provides access to the extensive work done by the applications teams through user guidelines and support provided by I/O specialists who work with system designers to optimize their clocking solutions.

Design Examples

The following three design examples reveal the value Xilinx serial connectivity design platforms deliver to widely divergent markets and applications. In each case, an FPGA with the appropriate combination of capacity, processing power, and transceiver performance provides the foundation for the platform, to which Xilinx adds IP and reference designs that target the particular application.

Serial I/O Solution for Wired Telecom Products

Wired telecommunications systems for the core, e.g., 8x10GE/2x40GE line card, place a premium on maximizing I/O performance and power density in the data plane while delivering cost-effective I/O implementations in the control plane. See Figure 7.



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Figure 7: 8x10GE/2x40GE Line Card

The example shown here is a 8x10GE/2x40GE line card with packet processing and traffic management. The line interface to 10G optics, MAC, and the packet processor are implemented using a Virtex-6 HX380T FPGA.

Virtex-6 HXT FPGAs provide all the capabilities required by the ultra-high-end designer to develop "green" products for the central office:

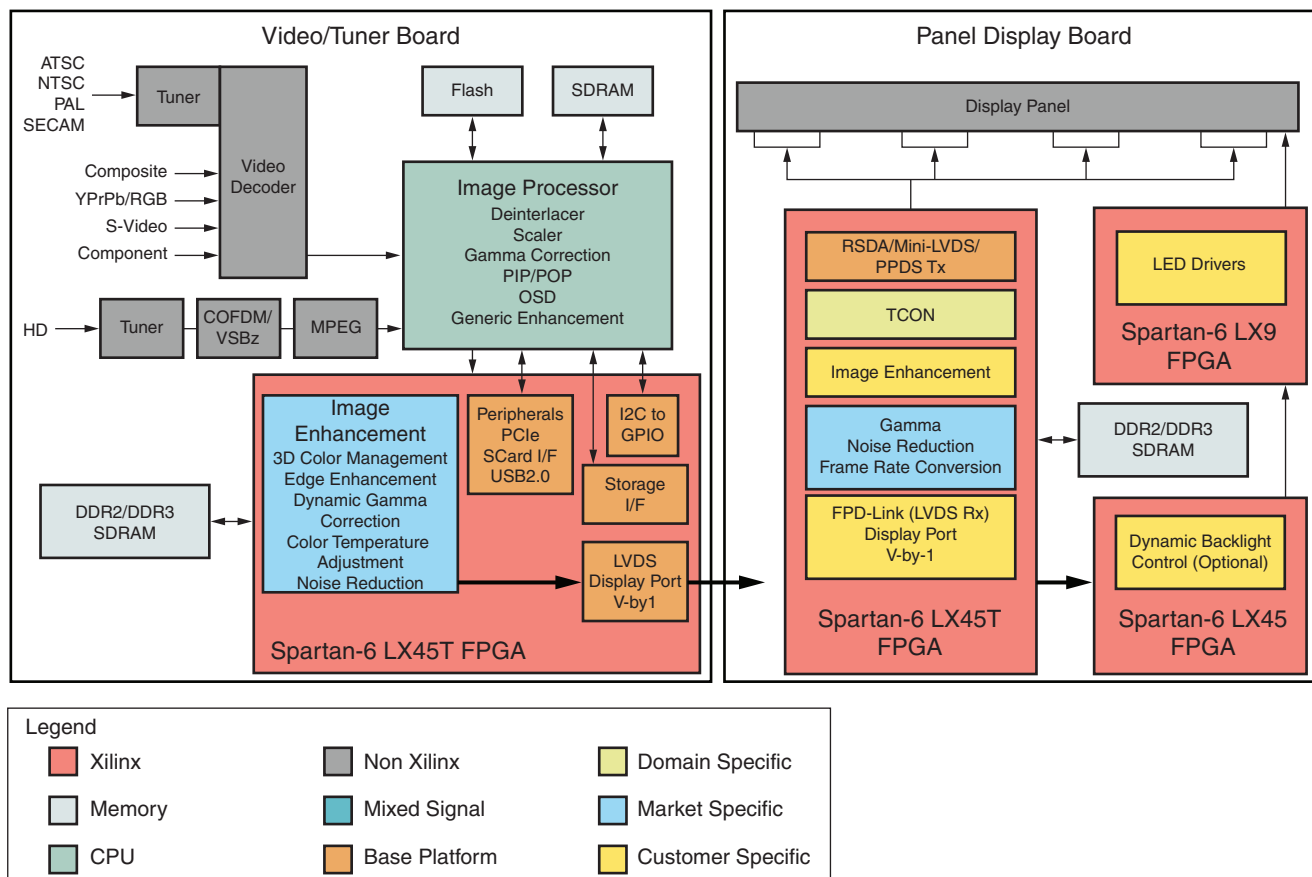
- Higher performance and bandwidth within existing power and cooling footprints
- Integrated packet-processing and traffic-management functions with faster and wider datapaths that satisfy tough throughput and latency requirements
- Simplified interfacing to DDR3, RLDRAM, and QDR SRAM with SelectIO technology
- 40G and 100G bridging implementations with IP for key protocols and flexible serial transceivers, supporting line rates above 10 Gb/s

The traffic management function is implemented using a Virtex-6 LX550T FPGA, which provides the necessary resources in terms of logic, 36 6.5 Gb/s GTX transceivers and 840 DDR3-capable I/Os. The lightweight Aurora protocol, ideal for chip-to-chip interfaces, connects the packet processor and the traffic manager, while the 100G Interlaken protocol provides a client-side interface through the backplane to the Network Processing Unit (NPU).

Virtex-6 FPGAs also integrate second-generation blocks for PCI Express that serve as the control plane interfaces. A Spartan-6 FPGA with an integrated block for PCIe 1.0 provides the reset controls and interface to system peripherals.

Serial I/O Solution for Consumer Products

Televisions are generally comprised of two printed circuit boards: the tuner and panel display boards. The tuner board accommodates the entire range of input standards and provides standard image processing and various custom image enhancement functions. The panel display board also performs a variety of image enhancement functions before delivering the data to the display. See [Figure 8](#).



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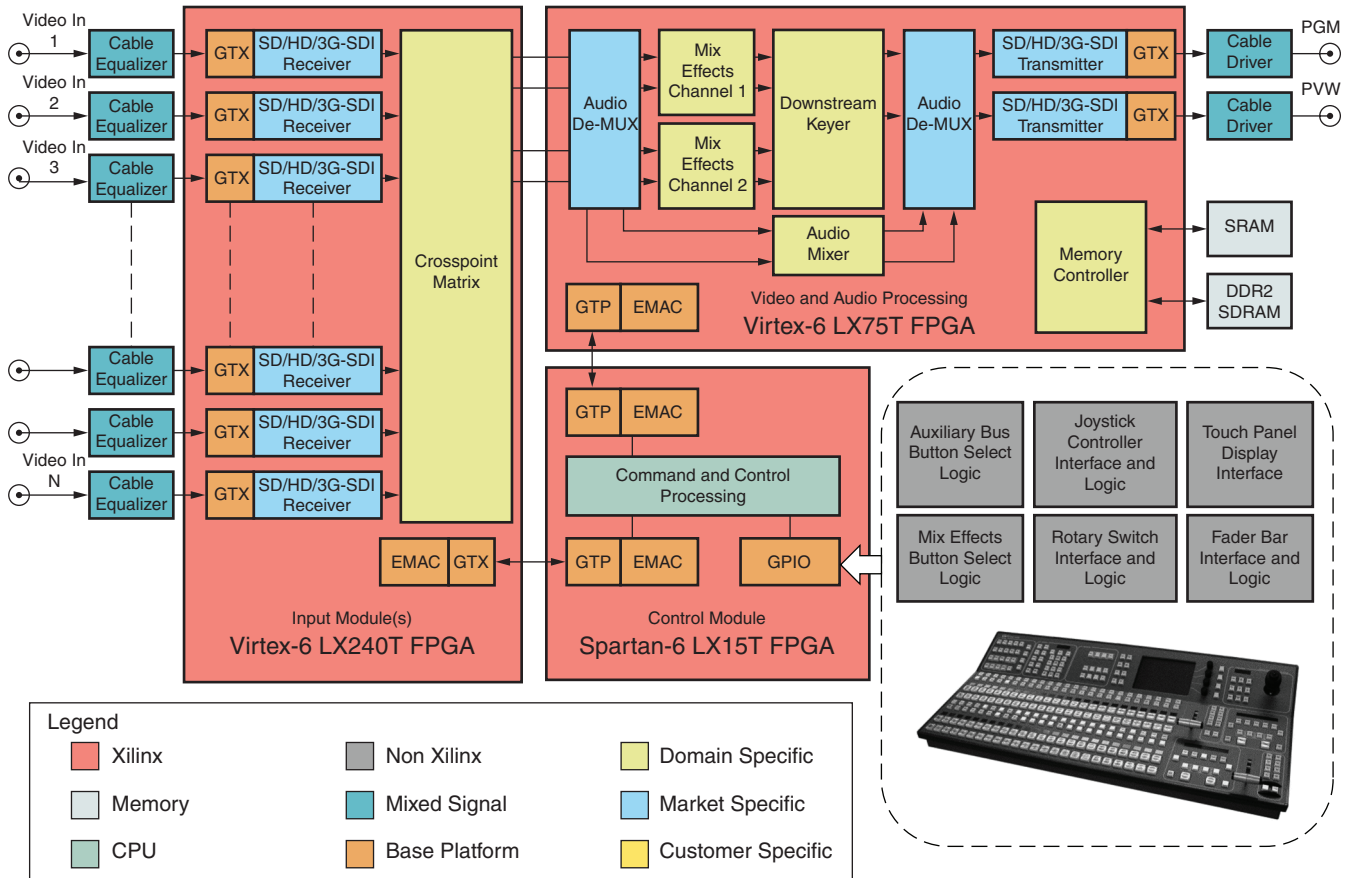
Figure 8: Tuner and Flat Panel Display Boards Require Faster I/O

Designs for this consumer (mainstream) application are naturally cost constrained, making the Spartan-6 LXT FPGA the appropriate foundation for the design platform. However, the most critical value afforded by the Xilinx connectivity platform is the speed with which the mainstream designer can deliver a differentiated solution to market. By providing a comprehensive set of IP, boards, and reference designs, the mainstream designer can move quickly through the creation of the necessary serial links, leaving more time to add differentiated value to the design.

Moreover, as higher resolutions (e.g., 4Kx2K), faster refresh rates (beyond 240 Hz) and new consumer display applications like 3DTV. creates massive increases in video data streams, these high-end TV designs will require faster serial I/O links. Xilinx design platforms provide the scalability and flexibility to accommodate the mainstream designer's product migration strategy in this market.

Serial I/O Solution for Video Broadcast Products

The production switcher is a state-of-the-art video broadcast system that provides especially critical value for live-event broadcasts. This system accommodates various input signal formats, switching these signals to an equally varied set of output formats that can have different resolutions, aspect ratios, and frame rates. See [Figure 9](#).



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Figure 9: Production Switcher Used for Video Broadcast

The core value for Xilinx design platforms serving this application begins with the increase in image (DSP and logic) processing performance achievable by Virtex-6 devices. Virtex-6 FPGAs also provide:

- Improved ratio of memory to DSP and logic
- More block RAM (improves video processing power and bandwidth capabilities and avoids having to move to larger parts just to get memory)
- Higher performance DSP blocks
- A pre-adder (improves filter speed, which, when combined with the Virtex-6 FPGAs maximum operation of 600 MHz, enables the design to handle more pixels and frames)
- As much as 30–40% lower dynamic power with speed and power trade-offs, an extremely attractive value in many parts of switcher designs
- Lower overall cost-per-channel when compared to previous generation solutions

Spartan-6 devices with their GTP transceivers offer a compelling video I/O solution for cost-sensitive, low-channel-count video switcher and router applications.

Conclusion

The ubiquity with which high-speed serial I/O has penetrated applications ranging from mainstream consumer devices to ultra-high-end equipment testifies both to the extreme amount of data all of these devices must handle—and given the right platform, the significantly easier facility with which even the novice can embrace the serial I/O design challenge.

Xilinx continues to invest heavily in the development of design platforms that extend this critical facility to its customers.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/15/09	1.0	Initial Xilinx release.

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