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Spartan-7 FPGAs: Meeting the Cost-Sensitive Market Requirements

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The Xilinx® Spartan®-7 family offers an array of low-cost, high-efficiency FPGAs. These devices have been purpose-designed to meet the special needs of the cost-sensitive market.

ABSTRACT

Spartan®-7 FPGAs bring together a high-performance 28nm programmable architecture with low-cost, small form-factor packaging, enabling high capability with a small PCB footprint.

The key advantages of the Spartan-7 family include:

- 28HPL process with highest performance per watt
- 28nm architecture scalability for design reuse
- Vivado® Design Suite for simple low-cost design entry and verification

This provides the designer with the necessary resources at low power and low total cost to meet the demands of cost-sensitive applications.

Introduction

The Xilinx® Spartan® FPGA family has earned its legacy as the leading cost-optimized FPGA class since its inception in 1998. It includes many generations of cost-optimized, small form-factor devices aimed at bridging, switching, controlling, processing, interfacing, and other functions. But to meet the performance and capabilities required by today’s cost-sensitive applications, e.g., the Industrial Internet of Things (I-IoT), Advanced Driver Assistance Systems (ADAS)/Driver Awareness Systems, and next-generation communications systems, requires much more than logic alone. With this increasing demand on functionality in a small footprint, the Spartan-7 family is designed to address the need for high-performance, cost-optimized, programmable logic available in a small-area footprint.

Choosing the Perfect Process

Xilinx developed the 28nm HPL process in conjunction with TSMC when creating the 7 series (Artix®-7, Kintex®-7, and Virtex®-7) devices. The high-K metal gate (HKMG) process provides the best combination of high performance and low power, enabling different families to be created to service different market needs. Spartan-7 FPGAs use the same 28HPL process as the established 7 series families and benefit from many of the same underlying architecture elements. The result is a family of compact, cost-optimized FPGAs that provide high logic and I/O performance with strictly controlled power consumption and able to fit into aggressively small form factor packaging—all at low cost. The flexibility of the process also enables the devices to operate at two different core voltages, enabling the user to make trade-offs between maximum performance and lowest power consumption. In contrast to the 28LP process used by competing FPGAs, the 28HPL process has a sufficiently wide operating window enabling devices to achieve a better performance/power metric—i.e., higher performance at lower power consumption. See Figure 1.

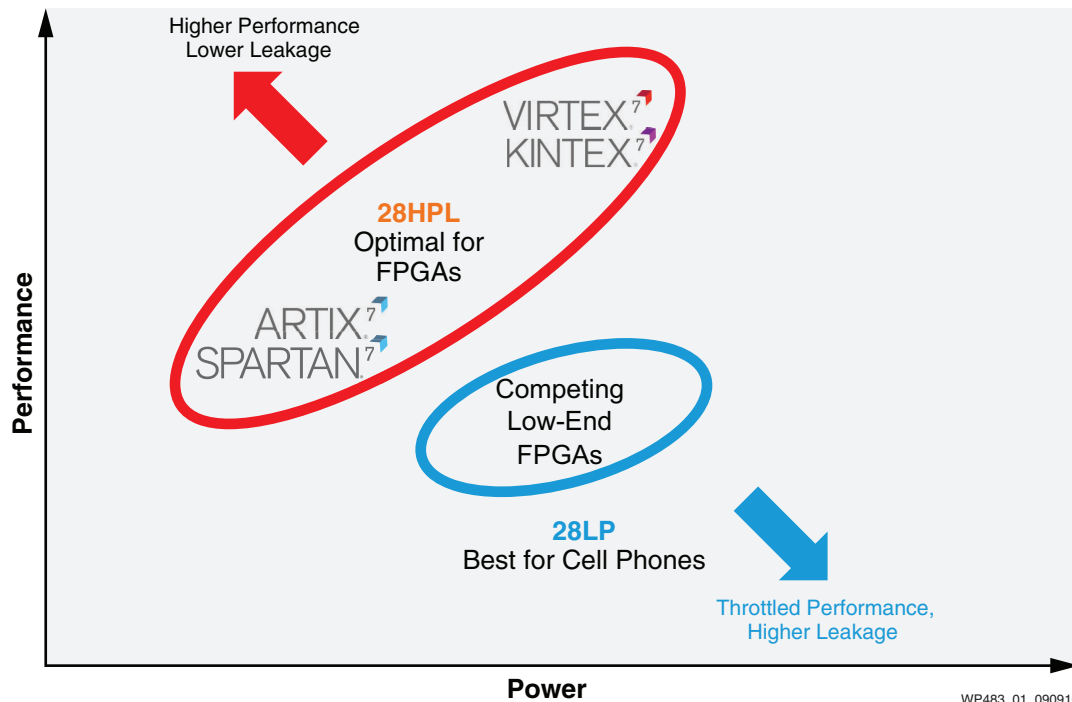
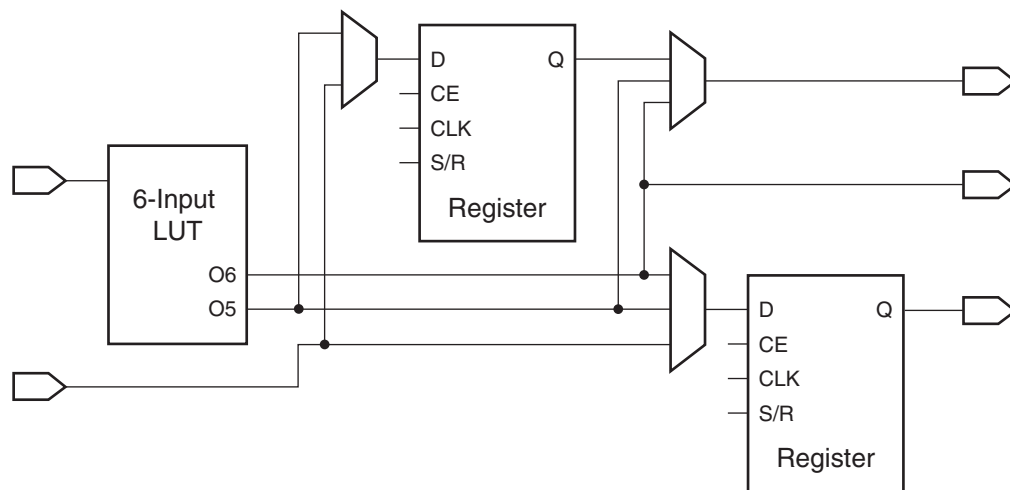


Figure 1: Spartan-7 FPGA 28HPL Process Advantages

Architected for Success

The logic structure is core to all FPGA architectures. Logic cells are referred to as a uniform measure of device capacity and capability, but for a designer to understand what can be done with a device, it is sometimes necessary to take a deeper look into the constituent building blocks. The Spartan-7 FPGA uses a configurable logic block (CLB) that contains slices that consist of look-up tables (LUTs), carry chains, and registers. These slices can be configured to perform logical functions, arithmetic functions, memory functions, and shift register functions.

Through the generations of Spartan-7 FPGAs, the quantity of resources within a CLB has evolved to continuously provide the optimum capability at the right cost. For example, the CLB in a first-generation Spartan device (late 1990s) contained one 3-input LUT, two 4-input LUTs, and two registers. Comparing that with the eight 6-input LUTs and sixteen registers in the CLB in the Spartan-7 FPGA, it is easy to see the progression in device capability. See [Figure 2](#).



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Figure 2: Spartan-7 FPGA LUT and Register Connections

LUTs in Spartan-7 FPGAs can be configured as one 6-input LUT with a single output or as two 5-input LUTs with separate outputs. Each LUT can be optionally registered in a flip-flop. Four LUTs and eight flip-flops form a slice, and two slices form a CLB. Some of the slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32).

These powerful and flexible features can all be implemented directly by the synthesis stage of the Vivado® Design Suite, enabling users to take advantage of advanced capabilities without needing to spend time learning all the individual port and signal names of the various blocks. The design efficiency offered by the Spartan-7 FPGA does not end with LUTs and registers, however; blocks dedicated to processing and storing digital signals are also made available to the designer.

DSP

Audio and video content is increasingly prevalent in modern systems. High-speed mathematical performance is required to enable the manipulation of digital audio and video data. To facilitate designing in such an environment, all Spartan-7 FPGAs include a number of DSP tiles, each containing two DSP slices. Each slice contains a 25x18 multiplier and a 48-bit accumulator capable of operating at frequencies of 550MHz or above. See [Figure 3](#).

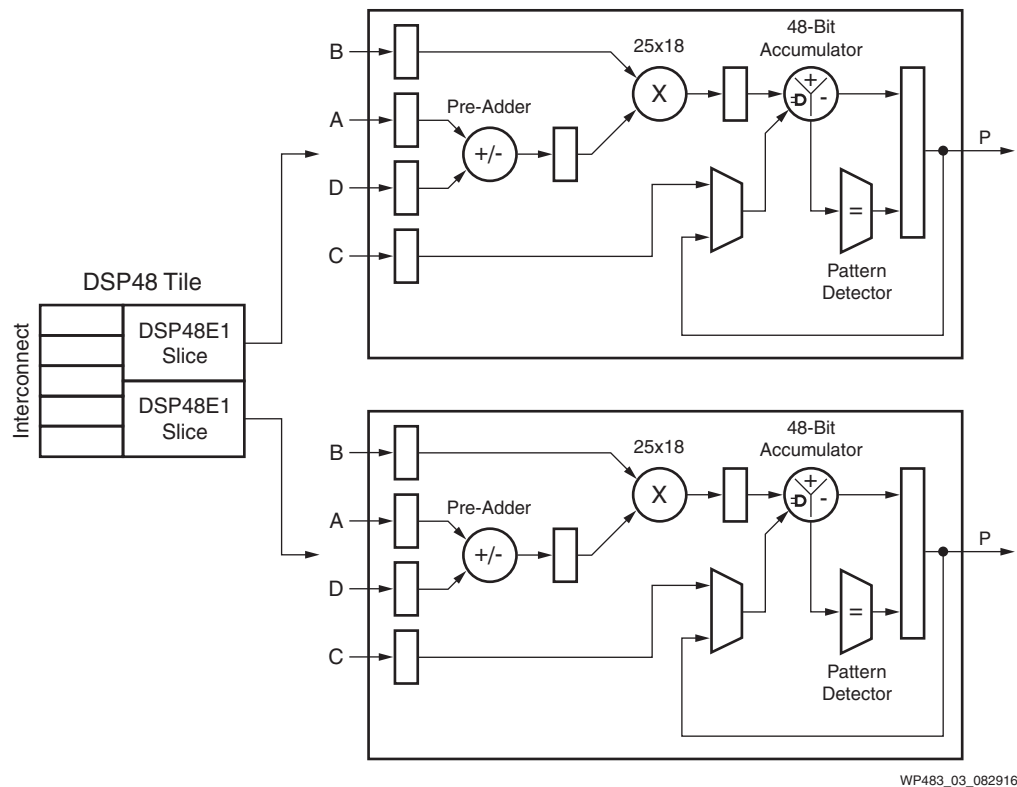


Figure 3: Spartan-7 FPGA DSP48 Tile

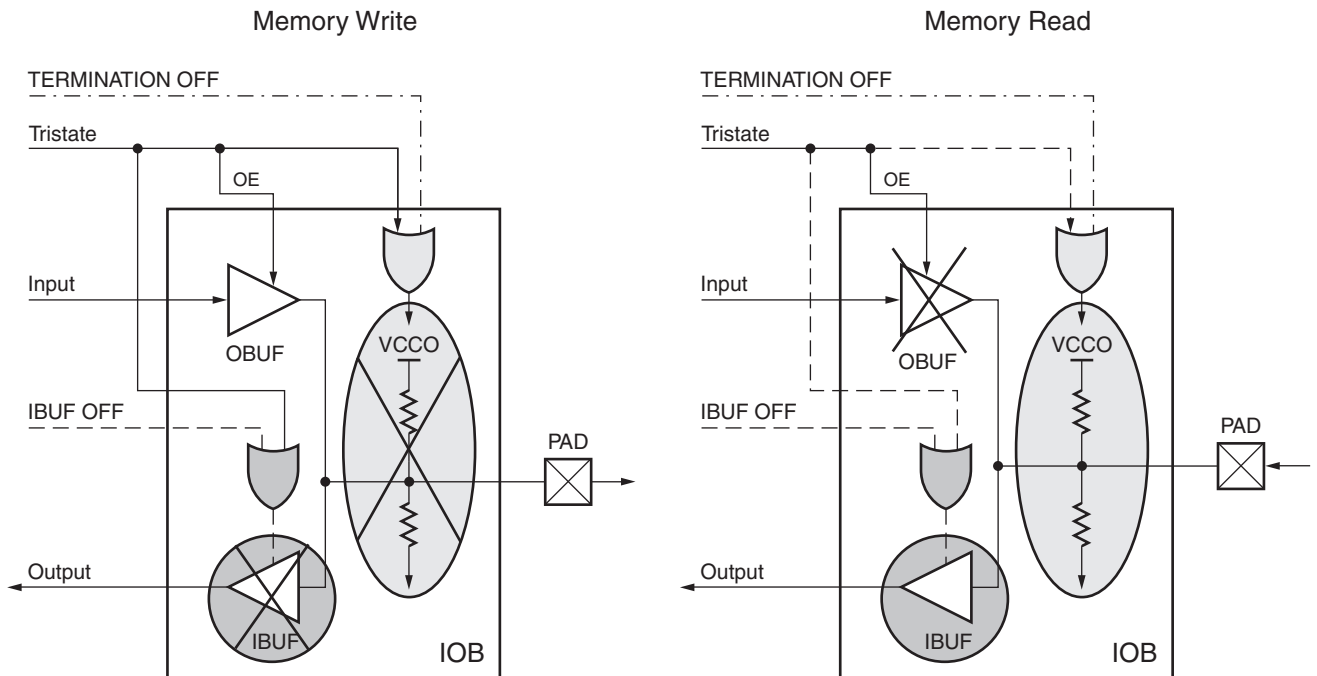
A 25-bit pre-adder enables resource-efficient creation of symmetrical filters such as FIR filters. Looking at a mid-density Spartan-7 device, such as the XC7S50, there are 120 DSP slices which, if all are used to implement symmetric FIR filters, provide the designer with 132 GMAC/s of processing power. Of course, with all this processing ability, the design also requires space to store pre- and post-processing data.

Memory

In addition to the distributed RAM mentioned earlier, all Spartan-7 FPGAs contain configurable 36Kb blocks of memory called block RAM. Each block RAM can support different modes of operation, including single-port, simple dual-port, true dual-port, and FIFO. The block RAM can be used as single 36Kb blocks, split into two independent 18Kb blocks, or connected together to make 64Kb or larger RAM. To ensure the contents of the memory is correct, each block RAM has optional error checking and correction (ECC) circuitry capable of correcting single-bit errors and detecting double-bit errors. Spartan-7 FPGAs contain up to 120 block RAMs, equating to 4.2Mb of on-chip storage. Add to this the distributed RAM, and the available storage rises to 5.3Mb.

I/O and Memory Interface

Spartan-7 FPGAs communicate across the PCB through their high-range (HR) I/O capable of communicating on many standards including HSTL, SSTL, LVDS, LVCMOS, and RSDS operating from 1.2V to 3.3V. Programmable drive strength enables the HR I/O to provide any-to-any connectivity up to 1250Mb/s while consuming as little power as necessary. To further reduce power, within the I/O block the individual components can be disabled when not used. For example, the output buffer is disabled during a read transaction and the input buffer is disabled during a write operation. See [Figure 4](#).



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Figure 4: Disabling I/O Buffers

Similar to the way in which other Spartan-7 FPGA features are enabled, the Vivado Design Suite relieves the designer of the complexity of deciding when to disable the I/O buffers.

The HR I/Os in Spartan-7 FPGAs are arranged in banks of 50 I/O pins. Due to implementation of a built-in memory PHY, every fully bonded bank is capable of implementing a memory interface. The memory interface generator (MIG) tool available in the Vivado Design Suite simplifies the creation of soft memory controllers to suit the designer's requirements. It can be configured to support up to 800Mb/s of low-cost, mainstream DDR3, or can alternatively support legacy standards such as DDR2 and LPDDR2. [Table 1](#) shows the Spartan-7 FPGA capabilities in table format.

Table 1: Spartan-7 Family Capabilities

Resource	Capability
Logic Cells	6K–102K
On-Chip Memory	0.2Mb–5.3Mb
Peak DSP Performance	11–176 GMAC/s
Peak I/O Data Rate	1250Mb/s
Peak Memory Interface Rate	800Mb/s

On the PCB

Applications such as industrial control systems often have electronics spread throughout a large area, but with a very limited area available at each location. Typically, signals from sensors need to be collated, processed, and sent to a central control unit to be combined together. The physical area available to perform the initial collation and processing is often very limited.

Small Form-Factor, Low-Cost Packages

To squeeze powerful programmable capabilities into space-limited locations, the Spartan-7 family employs a number of low-cost packages as small as 8x8mm with 0.5mm ball pitch. Devices available in the same package are always footprint-compatible, so it is possible for a user to migrate upwards within a single package if increased functionality is required.

XADC

Most Spartan-7 FPGAs contain a flexible analog interface called an XADC. When combined with programmable logic, the XADC can address a broad range of data acquisition and monitoring functions. This enables the designer to monitor system behavior even in remote, hard-to-access locations. See Figure 5.

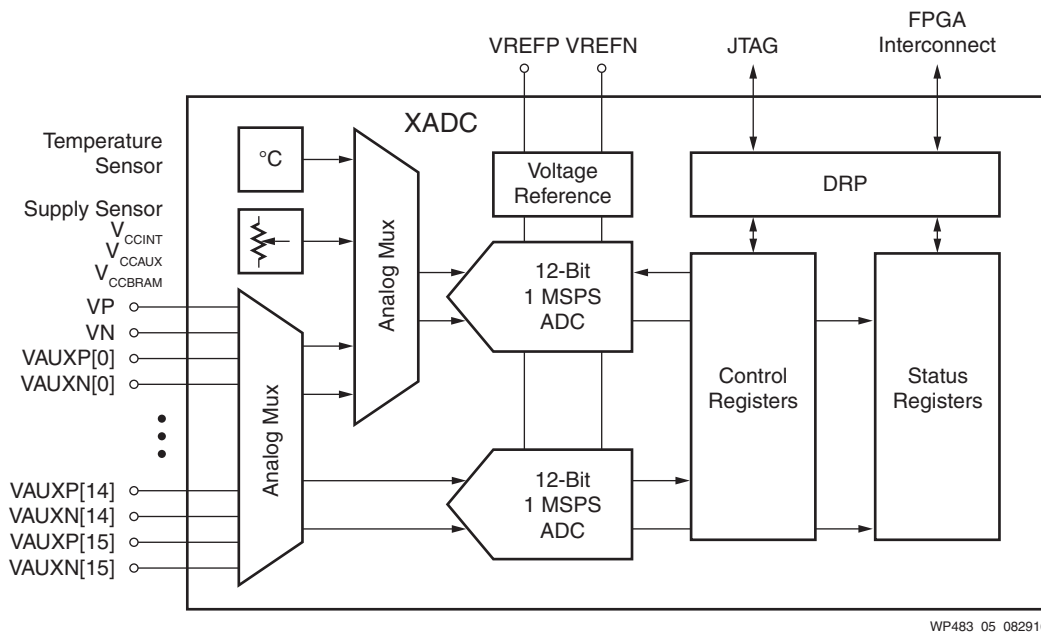


Figure 5: XADC Block Diagram

The XADC contains two 12-bit, 1MSPS ADCs with separate track and hold amplifiers, an on-chip multiplexer of up to 17 external analog inputs, and on-chip thermal and supply sensors for overall system reliability, availability, safety, and security enabling compliance to FIPS 140-2 security level 4.

Design Security

In addition to operational security provided by the XADC, most Spartan-7 FPGAs provide design and IP security through a number of different measures. The programming file, or bitstream, can be encrypted using 256-bit AES encryption to ensure confidentiality when the system is powered off and during power-on configuration. The decryption key can be stored in either battery-backed RAM or eFuse, with the former able to clear its contents of the key upon tamper detection.

Providing the Tools for the Job

Vivado IDE leads the way in providing simple, pushbutton design methodology with many advanced features to enable designers to quickly build designs targeting FPGAs and SoCs. Many design reuse features enable sections of the design or IP created for one device or family to be packaged for later reuse in another device or family that uses similar architecture. For example, a designer can create IP that is used in a Spartan-7 FPGA. As system requirements evolve, the designer can reuse that same IP in an Artix-7 FPGA.

The Vivado Design Suite allows the user to input RTL designs in the language of their choice with support for VHDL 2008, Verilog, and System Verilog. After the design is created, numerous debug and verification tools are available to ensure correct functionality, including a no-cost, mixed-language simulation tool with no code line limits.

All production Spartan-7 devices are supported by the free Vivado HL WebPACK™ Edition, providing the fastest and lowest-cost tooling for these devices.

Conclusion

Spartan-7 FPGAs bring together a high-performance 28nm programmable architecture with low-cost, small form-factor packaging enabling high capability with a small PCB footprint. A combination of logic, memory, DSP, I/O, and memory interface circuitry and the 28nm high-performance, low-power process enables Spartan-7 devices to perform demanding functions such as sensor interfacing, motor control, and protocol bridging. The established Vivado Design Suite provides numerous time saving features that allow designers to build complex cost-sensitive designs on Spartan-7 FPGAs with relatively little effort.

For more information, see www.xilinx.com/products/silicon-devices/fpga/spartan-7.html

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/27/2016	1.0	Initial Xilinx release.

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