

Next-Generation Zynq UltraScale+ RFSoc

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RFSoc



Agenda

Industry's only single-chip adaptable radio platform

High channel count with up to 50% power and footprint reduction



Now delivering up to 6GHz of direct-RF sampling

Flexible, multiband radio for 5G wireless, radar, cable access, and a breadth of RF-applications

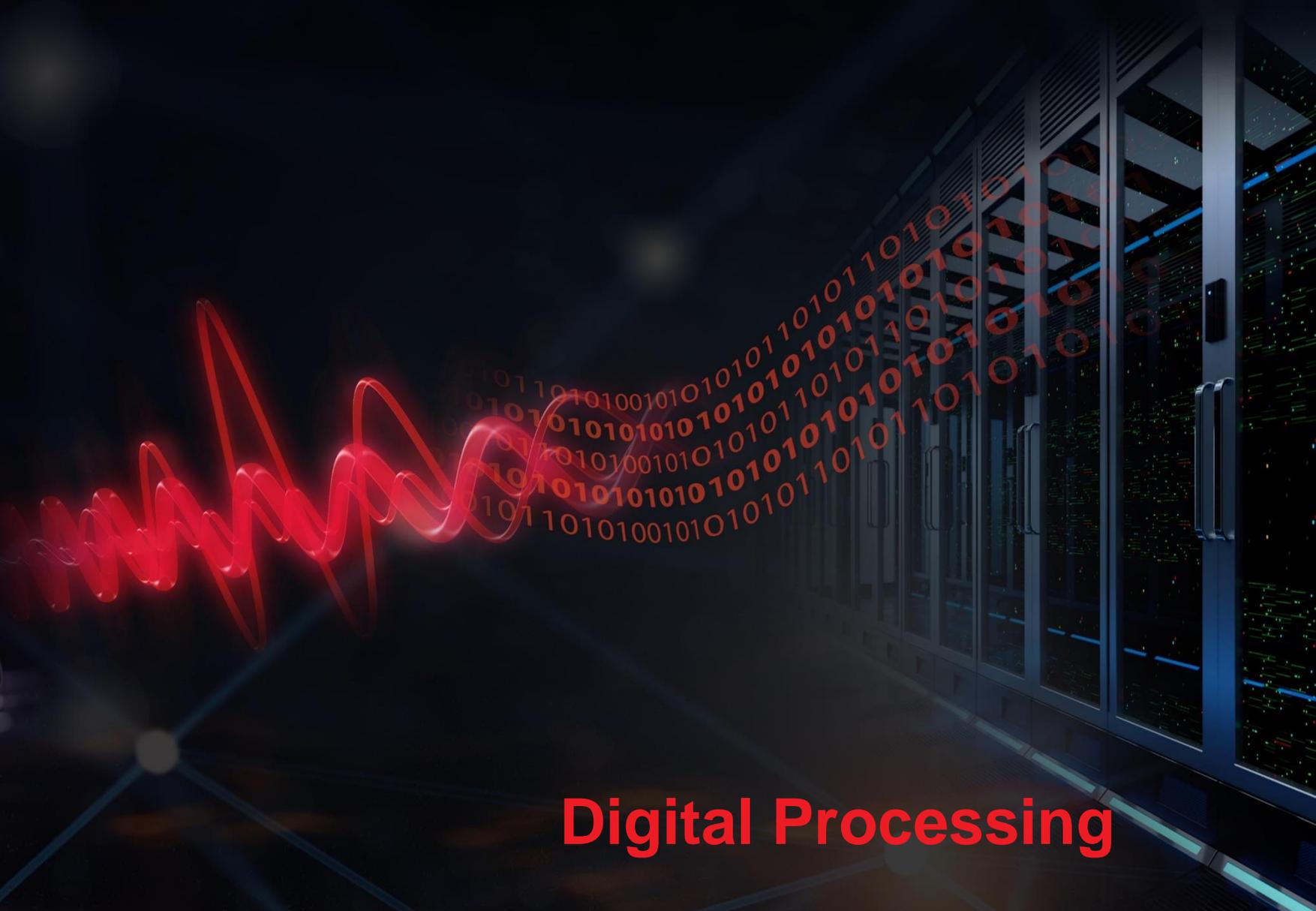
Xilinx is an RF-analog leader meeting current & future market needs

Keeping pace with market deployment needs and committed to integrated RF sampling

Analog World



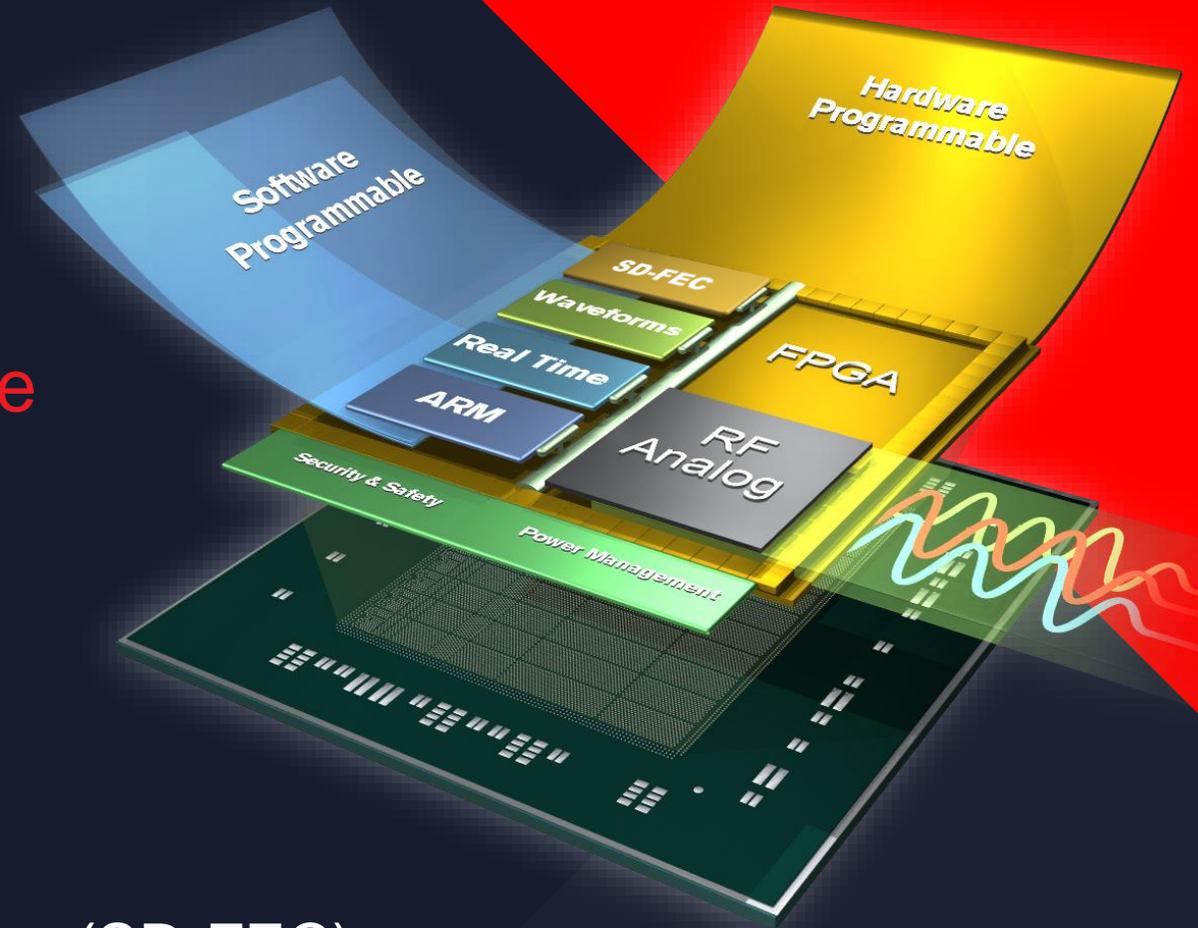
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Digital Processing

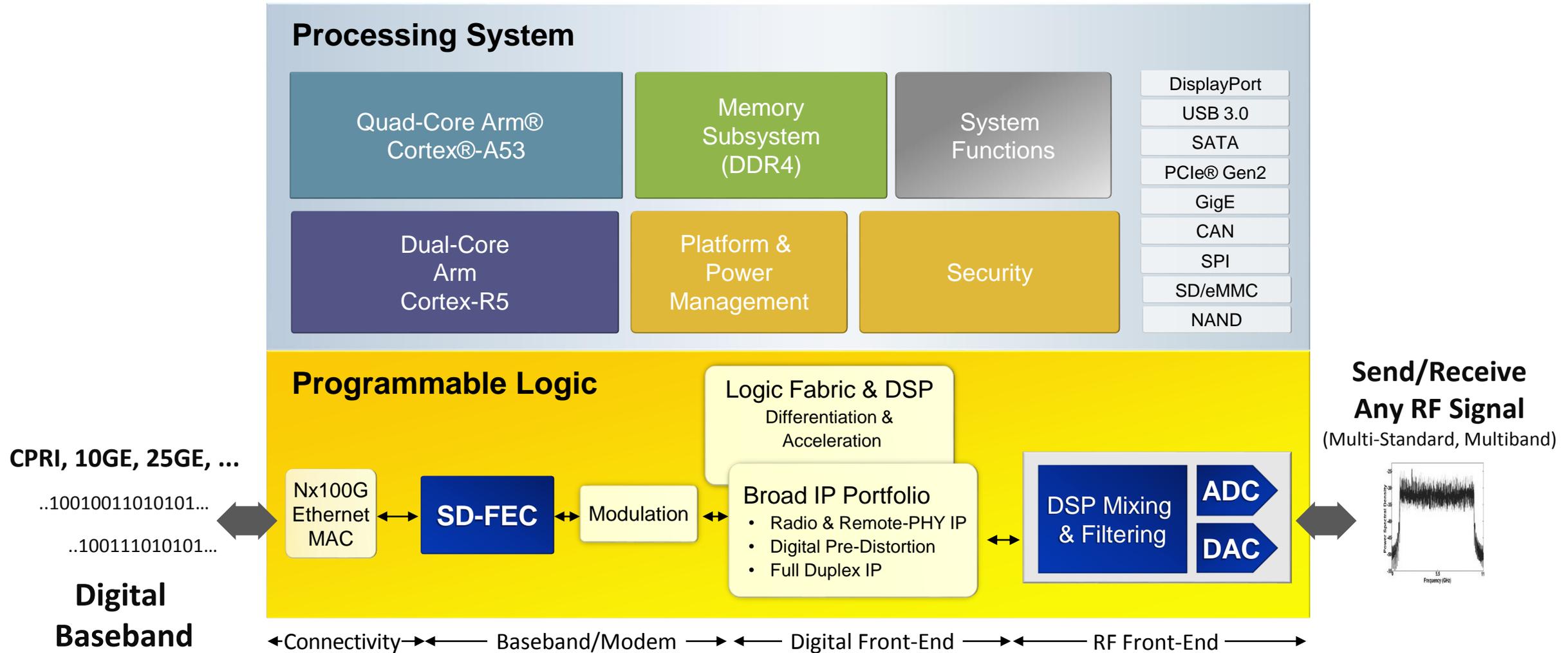
Zynq UltraScale+ RFSoc

The First Hardware Programmable
RF System-on-Chip (RFSoc)



- ✓ Integrated RF-Class Analog
- ✓ Soft-Decision Forward Error Correction (SD-FEC)

Single-Chip Adaptable Radio Platform



Integrating the RF Signal Chain

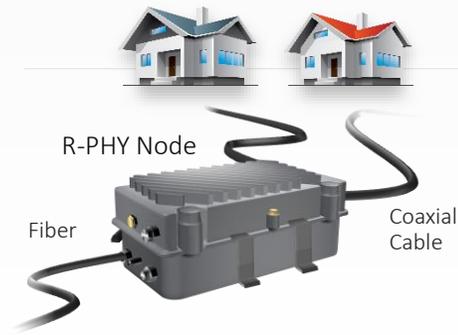
Key Target Markets and a Breadth of RF-Applications

Wireless



- > Power & Footprint for mMIMO
- > LDPC for 5G Baseband
- > IF Digital Transceiver for mmWave 5G NR

Cable-Access Remote-PHY Node



- > Single-Chip Solution for DOCSIS 3.0 and 3.1
- > Supports Extended Spectrum DOCSIS
- > Adaptable HW for Future-Proofing

Phased Array Radar



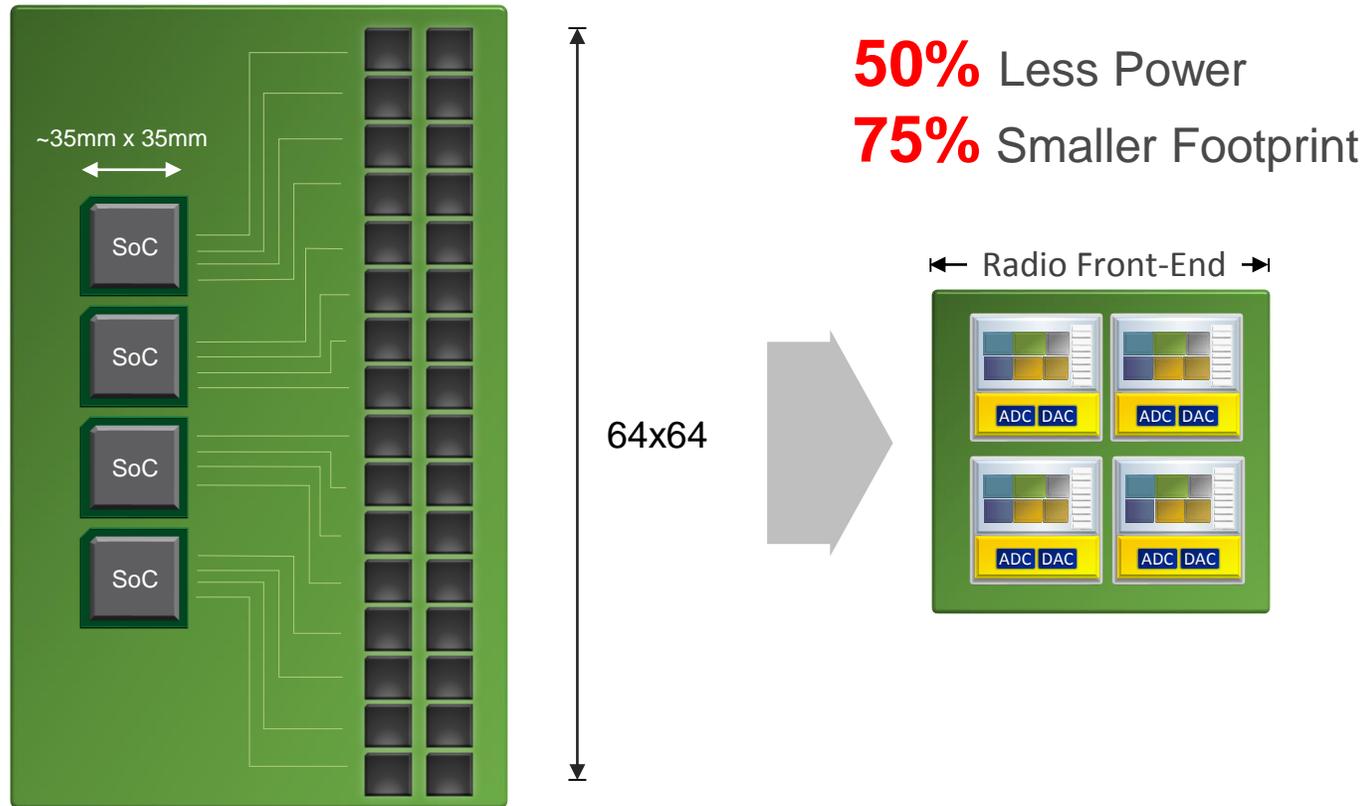
- > SW & HW Reconfigurable
- > Full L-Band & S-Band Sampling
- > Partial C-Band Direct Sampling

Breadth of RF-Applications



- > LiDAR Systems in Automotive
- > Test & Measurement
- > Satellite Communications

Massive MIMO Radios Developed by Tier-1 Wireless Network Provider



50% Less Power
75% Smaller Footprint

Customer Problem

Implementing 64x64 mMIMO requires up to 9X more IC components

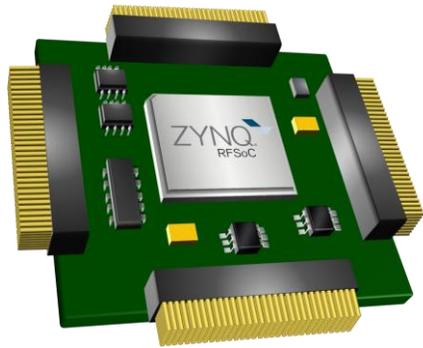
Xilinx Solution & Differentiation

- > Four Zynq® UltraScale+™ RFSoCs
- > IC count reduced from 36 to 4
- > Significantly less power and footprint

Xilinx System Content Increased by Over 35%

Modularity for Large-Scale Multi-Function Phased-Array-Radar (MPAR) Systems

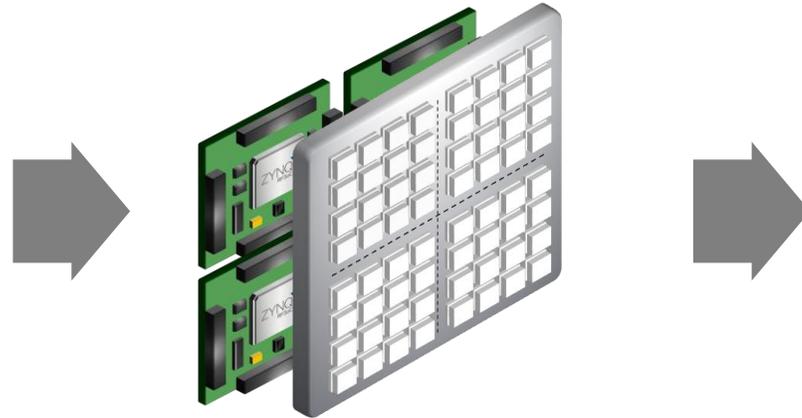
Single-Chip
16x16 TRX Module



Rockwell
Collins



Four ZU+ RFSoc
TRX Modules
per 64x64 TRX Panel



Common Module for Diverse
MPAR Systems



Next-Generation Zynq UltraScale+ RFSocCs

Greater Performance, Flexibility, and Integration



Portfolio Aligned with Market Requirements

2018



GEN 1

Analog Bandwidth

2019



GEN 2

Analog Bandwidth

2020



GEN 3

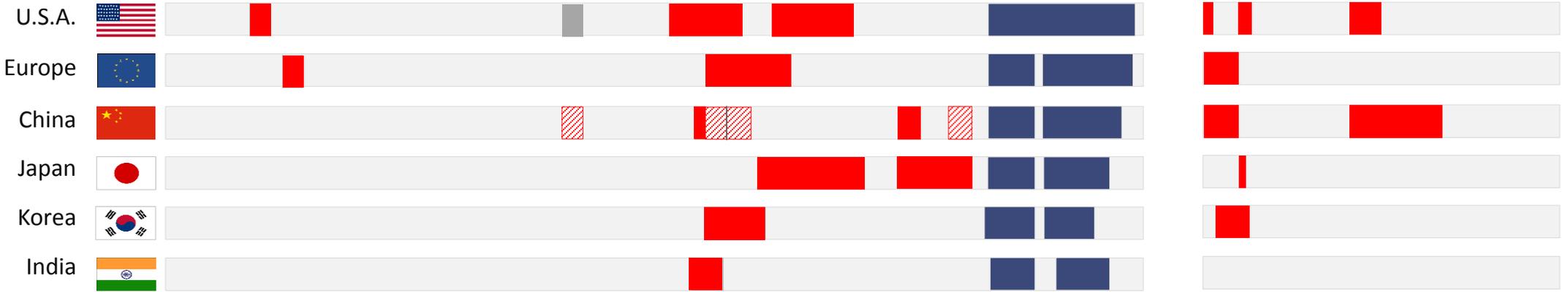
Analog Bandwidth

IF Implementation (All Devices)

- Licensed 5G Bands █
- Recently Allocated 5G Band █
- Unlicensed 5G Bands █
- Existing Bands █

1GHz 2GHz 3GHz 4GHz 5GHz 6GHz 24GHz 52.6GHz

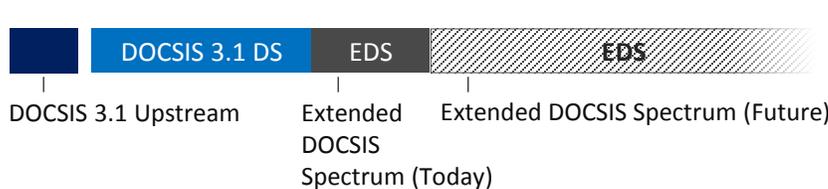
5G



Phased Array Radar



Cable Access Remote-PHY



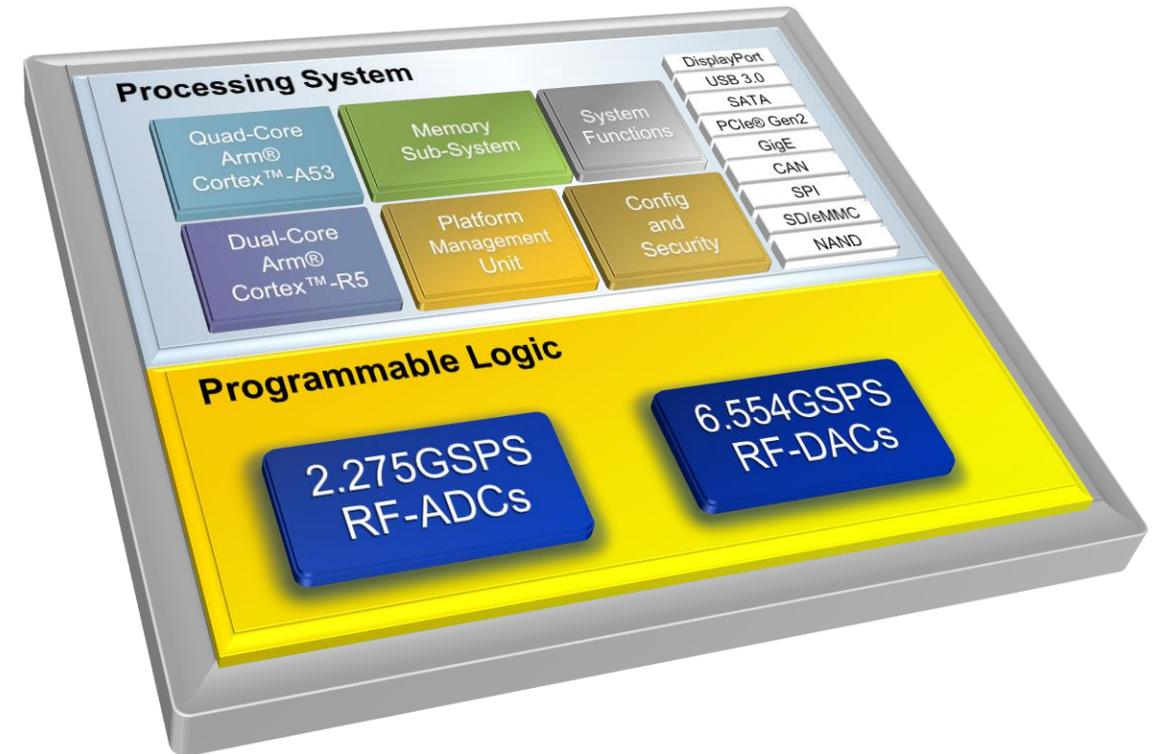
Introducing Zynq UltraScale+ RFSoc Gen 2

Meets timelines for 5G NR bands in Asia

- > Engineering Samples: NOW
- > Production: June 2019
- > Demo at MWC 2019

Enhancements

- > Greater RF performance for 16x16 configuration
- > Scalable from base portfolio 16x16 device



Introducing Zynq UltraScale+ RFSoc Gen 3

Extended RF performance for more use cases

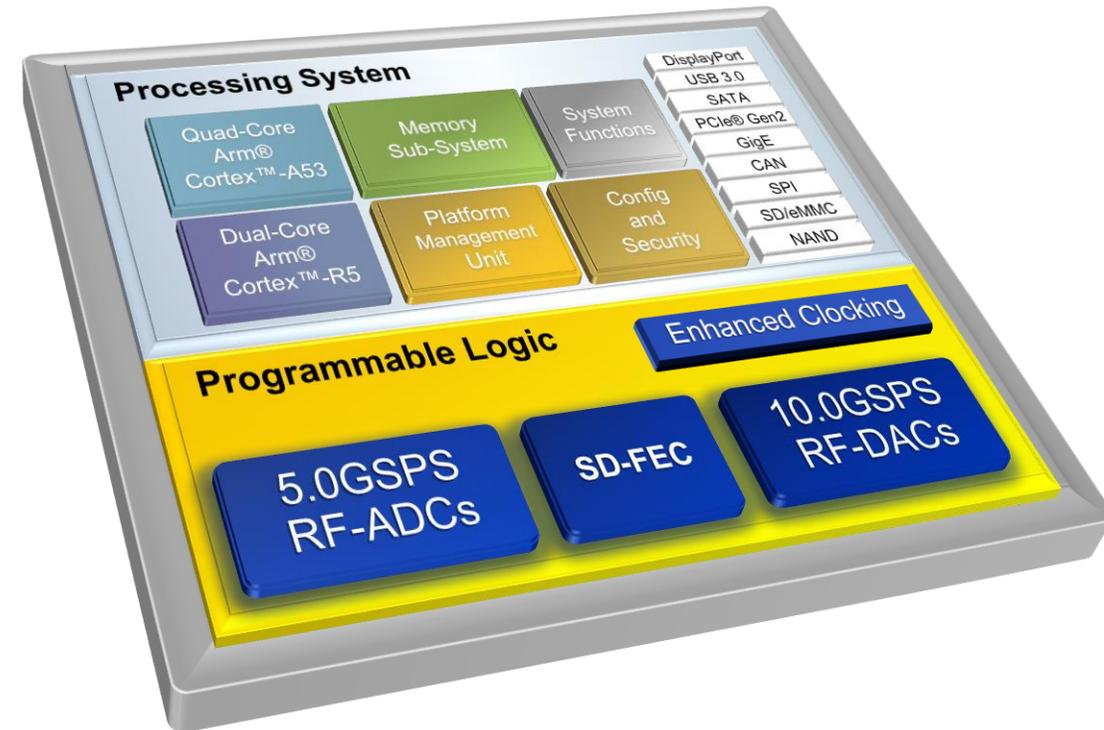
- > Full Sub-6GHz Direct-RF support
- > 14 bit performance
- > Up to 20% power reduction in RF-DC for TDD use case
- > Extended mmWave interfacing

Reduced BOM and system cost

- > Enhanced clocking distribution simplifies PCB board design
- > Eliminates onboard clocking component cost

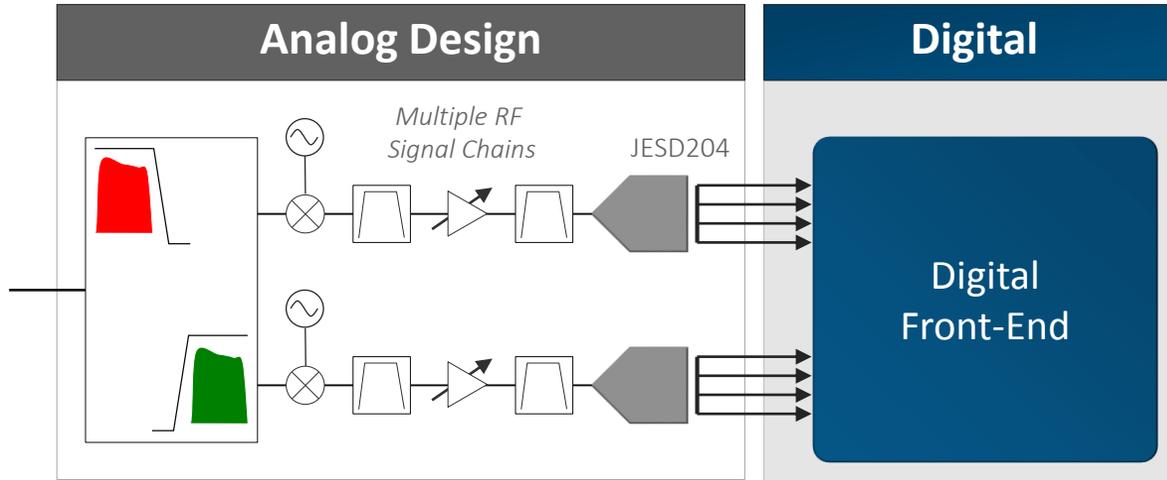
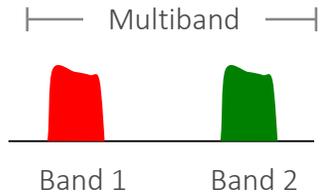
Simplified design and greater flexibility

- > Full multiband, multi-standard support
- > Additional interpolation and decimation simplifies frequency planning

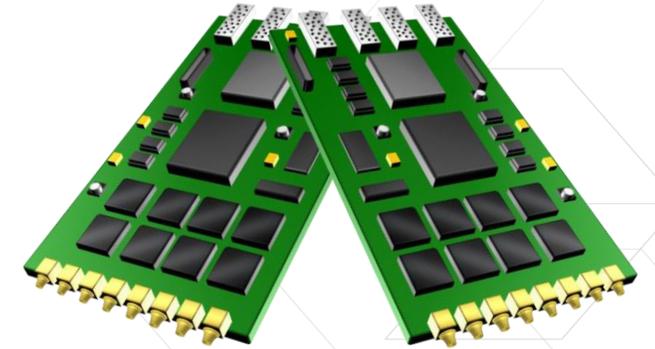


Multiband, Multi-Standard Reconfigurable Platform

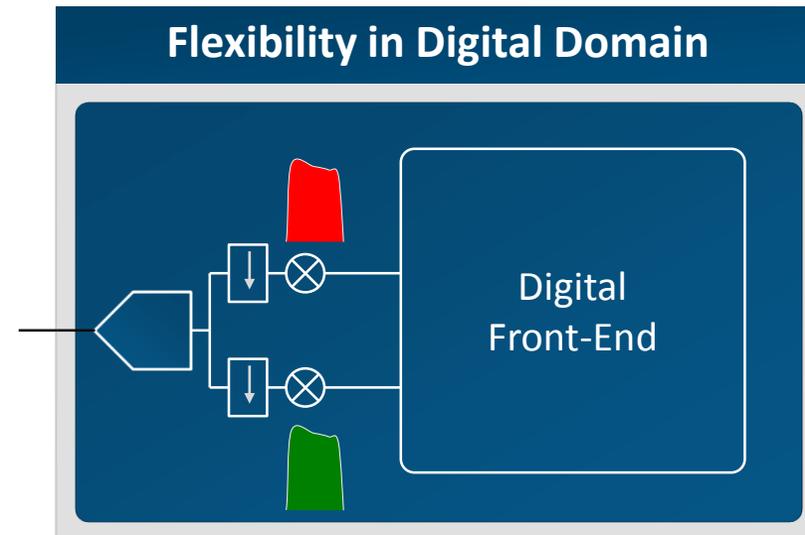
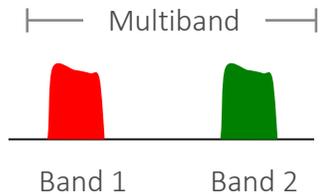
Complex RF Signal Chains



Multiple Platforms
for Different Radio Configurations



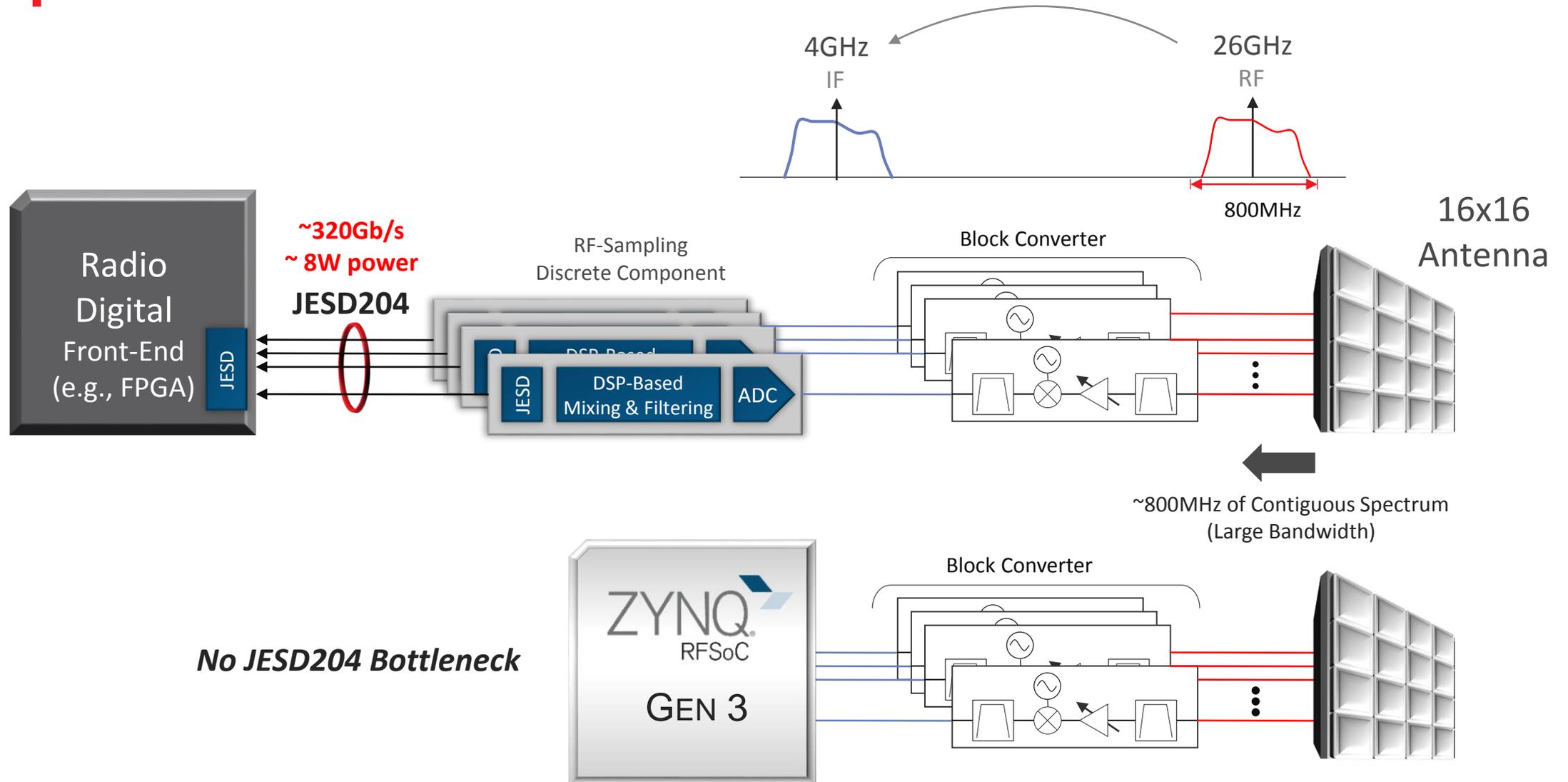
Complex RF Signal Chains



Single Platform
Multiband Reconfigurable



Extended Intermediate Frequency (IF) Implementation for mmWave



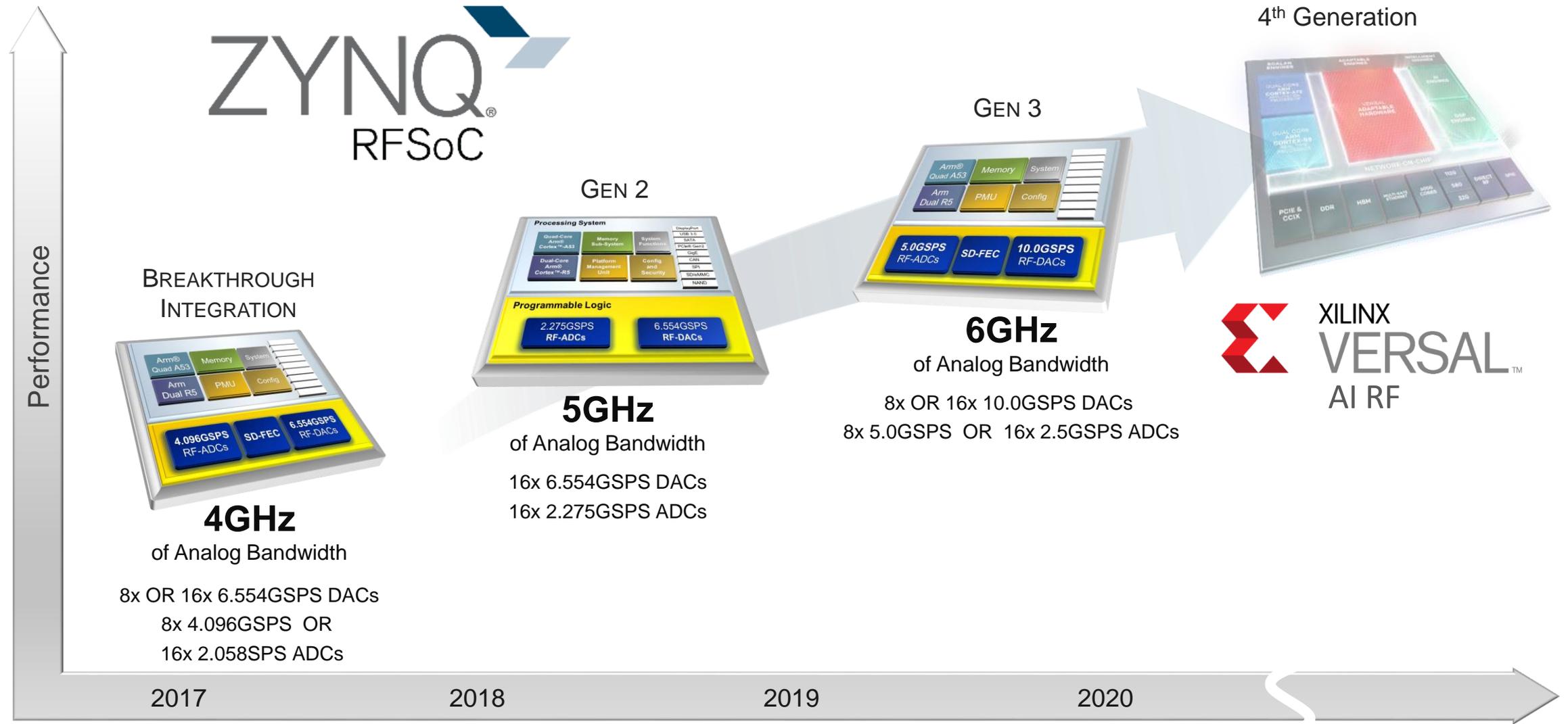
Zynq UltraScale+ RFSoc Gen 2 & Gen 3 Product Table

		Gen 2	Gen 3			
		n79 5G NR Bands	FDD/DPD Feedback	Radar & Fixed Wireless	DOCSIS & Backhaul	Radar & Fixed Wireless
		Radio			Access	Radio
		ZU39DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
Analog-Digital Signal Chain	14-bit, 5.0GSPS ADC	-	4	8	8	-
	14-bit, 2.5GSPS ADC	-	8	-	-	16
	12-bit, 2.275GSPS ADC	16				
	14-bit, 6.554GSPS DAC	16				
	14-bit, 10GSPS DAC	-	12	8	8	16
	SD-FEC	-	8	-	8	-
Processing System & Programmable Logic	Application Processor Core	Quad-core Arm Cortex-A53 MPCore® up to 1.33GHz				
	Real-Time Processor Core	Dual-core Arm Cortex-R5 MPCore up to 533MHz				
	High Speed Connectivity	DDR4-2666, PCIe Gen3 x16, 100G Ethernet (PCIe Gen4 x8 for Gen 3 ZU+ RFSoc)				
	Logic Density (System Logic Cells)	930K	930K	930K	930K	930K
	DSP Slices	4,272	4,272	4,272	4,272	4,272
	33G Transceivers	16	16	16	16	16

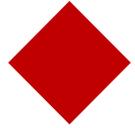
Roadmap



Roadmap to Meet Current and Future Market Needs



Summary



Zynq UltraScale+ RFSoc base devices in full production with multi-market success

- > 4GHz of analog bandwidth
- > Industry recognized with multi-market success in wireless, cable access, and radar
- > A growing ecosystem of boards, tools, and IP



Zynq UltraScale+ RFSocs Gen 2

- > 5GHz of analog bandwidth
- > Timely support of the latest 5G bands for regional deployment
- > Sampling NOW. Production release in June 2019



Generation Zynq UltraScale+ RFSocs Gen 3

- > 6GHz of analog bandwidth for full direct-RF support of sub-6GHz bands, extended millimeter wave interface
- > Full multi-band support
- > Simplified clocking, more decimation, and interpolation options

Scalability and migration across the portfolio

Adaptable.
Intelligent.



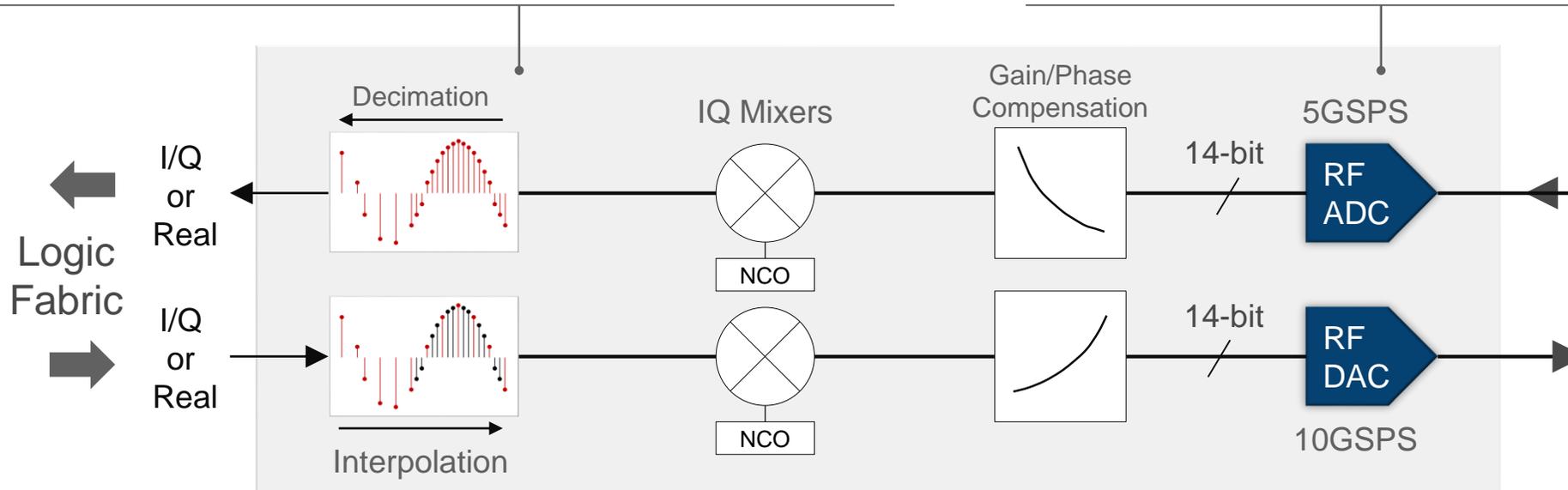
Enhanced DSP & Data Converters

Enhanced DSP Mixing and Filtering

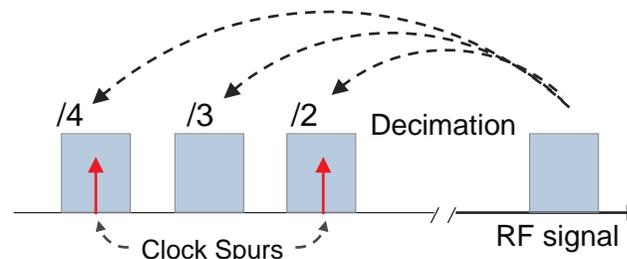
- > Additional interpolation/decimation for RF flexibility/freq. planning
- > (1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x)
- > Offloads DSP processing (filtering) from programmable logic

6GHz Direct RF Bandwidth

- > 14-bit 5GSPS ADCs, 14-bit 2.5GSPS ADCs
- > SW programmable RF signal chain up to 6GHz
- > Optimal mix of ADCs for 8x8 FDD Implementations (Wireless)



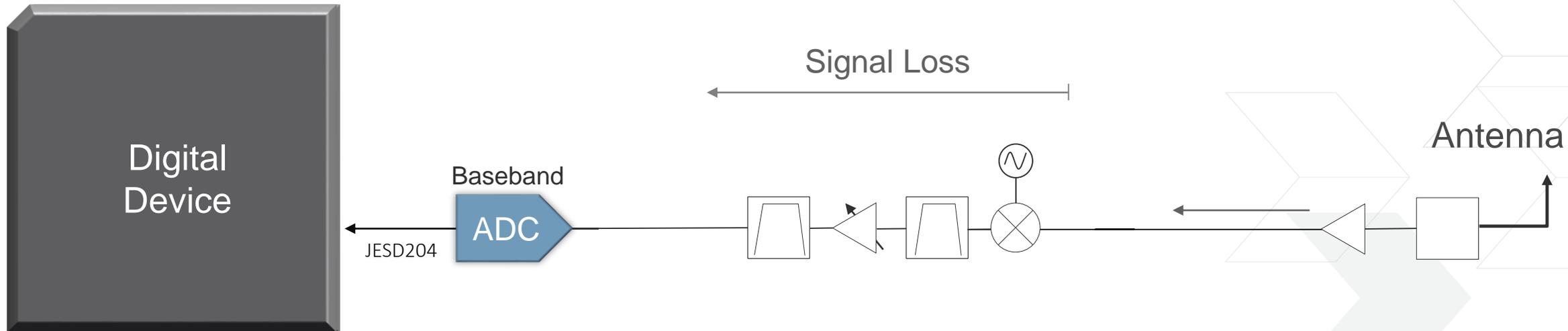
Enhanced DSP Mixing and Filtering



Platform Flexibility with Direct RF-Sampling

Traditional IF (*Intermediate Frequency*) Sampling

Signal conditioning **before** ADC sampling using **analog** components



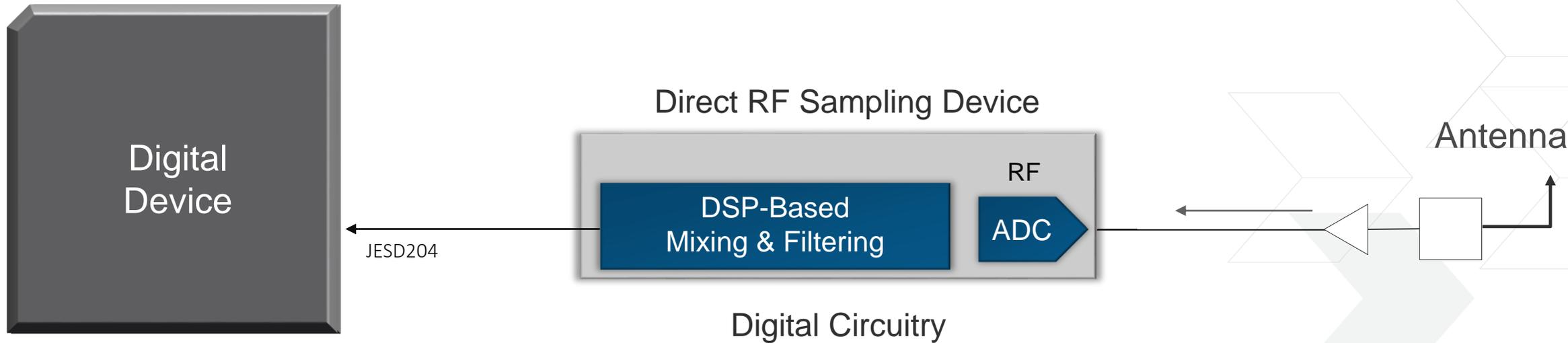
Analog-Based Signal Conditioning

- ✓ Power efficient
- ✗ Greater footprint due to multiple components
- ✗ Greater design effort due to BOM complexity
- ✗ Limited flexibility due to fixed components

Platform Flexibility with Direct RF-Sampling

Direct RF Sampling

Signal conditioning **after** ADC sampling, in the **digital** domain

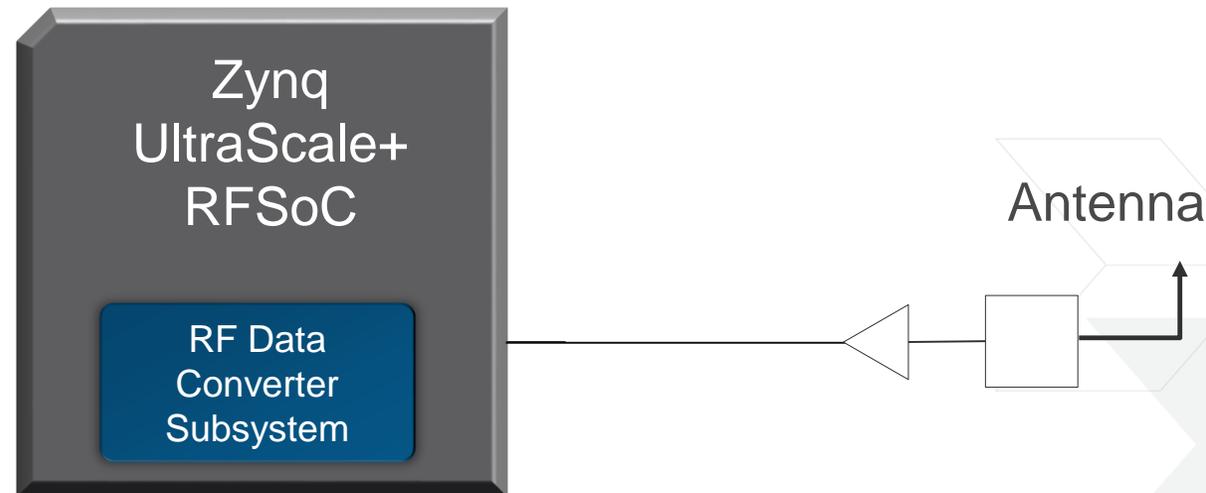


- ✗ Higher power → higher sample rate
- ✗ Significant footprint → discrete component
- ✗ BOM complexity → discrete component
- ✓ Flexibility in the digital domain

Platform Flexibility with Direct RF-Sampling

Direct RF Sampling

Signal conditioning **after** ADC sampling, in the **digital** domain



- ✓ Lower power through integration
- ✓ Smaller footprint through integration
- ✓ Faster design cycle with less BOM complexity
- ✓ Flexibility in the digital domain

Scalability Across the Portfolio

		Gen 1					Gen 2	Gen 3 (FDD Support)						
		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR			
Radio		●	●	●	●	●	●	●	●	●	●			
Backhaul				●										
Baseband		●												
Fixed Wireless Access				●	●	●		●		●				
Cable R-PHY				●					●					
Satellite / Test & Measurement			●			●		●			●			
Radar / SIGINT					●			●			●			
		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR			
Analog Signal Chain	RF Data Converter Subsystem	RF-ADC w/DDC	# of ADCs	-	8	8	8	16	16	8	4	8	8	16
			Max ADC rate (GSPS)	-	4.096	4.096	4.096	2.058	2.275	2.5	5.0	5.0	5.0	2.5
			Resolution (bits)	-	12	12	12	12	12	14	14	14	14	14
		RF-DAC w/DUC	# of DACs	-	8	8	8	16	16	12	8	8	16	
			Max DAC Rate (GSPS)	-	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	
			Resolution (bits)	-	14	14	14	14	14	14	14	14	14	
		SD-FEC	8	-	-	8	-	-	8	-	8	-		
RF input Freq max. GHz			4			5		6						
Decimation / Interpolation			1x, 2x, 4x, 8x			1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x							
Programmable Logic (PL)	Integrated IP	System Logic Cells (K)	930	678	930	930	930	930	930	930	930	930		
		DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272		
		GTY Transceivers	16	8	16	16	16	16	16	16	16	16		
		PCIe® Gen 3x16	2	1	2	2	2	2	2	2	2	2		
		100G Ethernet w/RS-FEC	2	1	2	2	2	2	2	2	2	2		
Package Footprint	D1156	35x35	■											
	E1156	35x35		■	■	■	■	■	■	■	■			
	G1517	40x40		■	■	■	■	■	■	■	■			
	F1760	42.5x42.5					■	■	■	■	■			
	H1760	42.5x42.5						■			■			

Zynq UltraScale+ RFSoc Results for the Latest 5G Bands

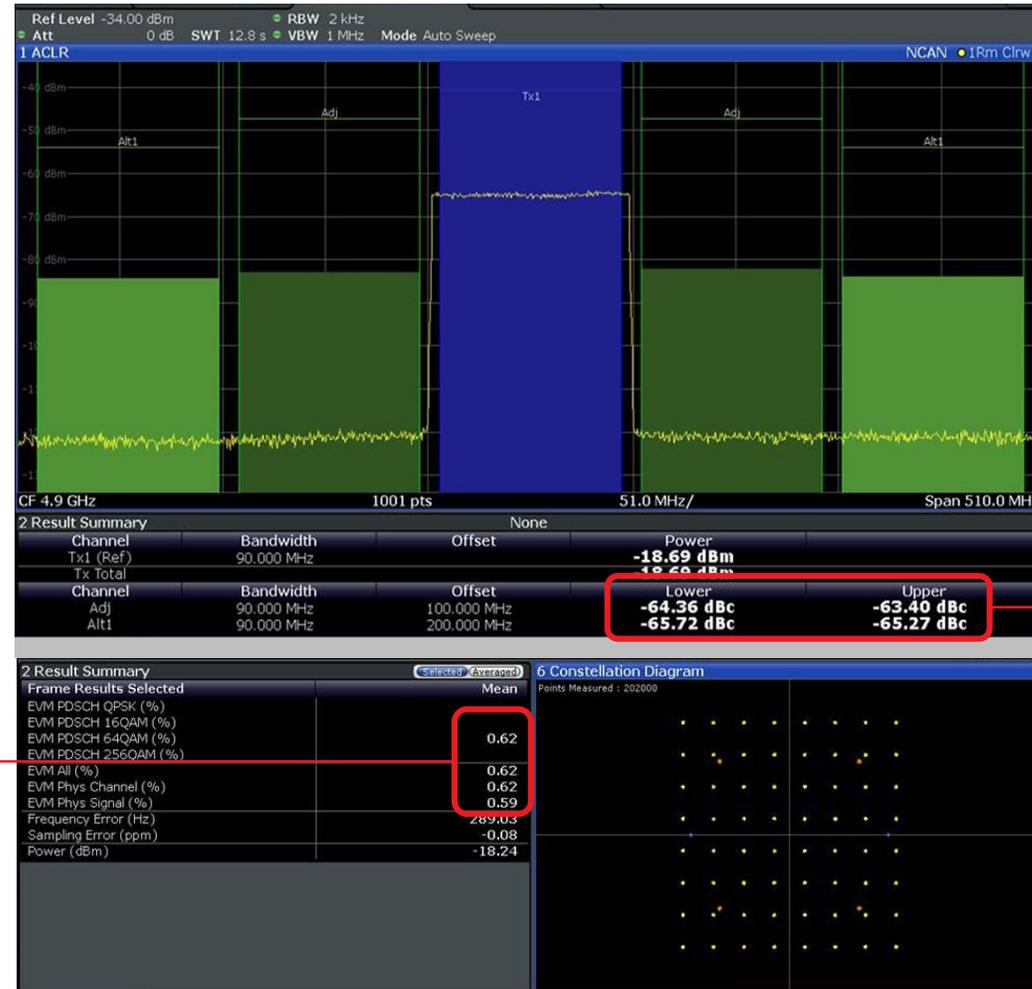
ZU39DR supporting 5G NR band n79 with Direct RF

> 5G NR n79 $F_{OUT} = 4.9GHz$

- >> 100MHz 64QAM waveform
- >> Internal PLL
- >> DAC mode = 32mA
- >> SCS = 30KHz
- >> $F_S = 5.898GSPS$
- >> Internal PLL – $F_{REF} = 491.52MHz$
- >> DAC in 32mA mode

> Measured Results

- >> $F_{OUT} = 4.9GHz$
- >> ADJ / ALT Channel < -63dBc
- >> EVM ~0.6%



EVM
~ 0.6%

ACLR
< -63dBc