

## **Spartan-7 SP701 FPGA Demonstration**

### Introduction

This step-by-step guide will show how to rapidly prototype an embedded system, using the Spartan-7 FPGA SP701 evaluation board.

We'll cover two applications using Vivado, a Xilinx tool for implementation and analysis of HDL and IP Integrator designs and Vitis, that enables the development of embedded software and accelerated applications on Xilinx platforms such as FPGAs, SoCs, and ACAPs.

Applications are:

- 1. Hello World application using MicroBlaze.
- 2. Pulse Width Modulation (PWM) application.





## Hello World application using MicroBlaze.



## Launch Vivado 2021.1

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VIVADO. ML Editions	<b>٤</b> XILINX.
Quick Start Create Project > Open Project > Open Example Project >	
Tasks Manage IP > Open Hardware Manager > Vivado Store >	
Learning Center Documentation and Tutorials > Quick Take Videos > What's New in 2021.1 >	
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## On the Vivado Quick Start page, select "Open an example project"

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## From the project templates, select "MicroBlaze Design Presets" and click "Next"





### Then enter the project name and location and click "Next"

🝌 Open Example P	roject		$\times$
Project Name			
Enter a name for yo	ur project and specify a directory where the project data files will be stored		<b>*</b>
Project name:	PWM_MicroBlaze		8
Project location:	C:/Xilinx/Projects		⊗ …
Create project	t subdirectory		
Project will be cr	eated at: C:/Xilinx/Projects/PWM_MicroBlaze		
?		< <u>B</u> ack <u>N</u> ext > <u>F</u> inish	Cancel



### Select the board to target "SP701"

#### 🝌 Open Example Project

#### Default Part

Choose a default Xilinx board for your project.

lisplay Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT Eleme
Kintex-UltraScale KCU105 Evaluation Pla		xilinx.com	1.7	xcku040-ffva115	1156	1.0	520	242400
Kintex UltraScale+ KCU116 Evaluation P		xilinx.com	1.5	xcku5p-ffvb676	676	1.0	280	216960
Virtex-UltraScale VCU108 Evaluation Pla		xilinx.com	1.7	xcvu095-ffva210	2104	1.0	832	537600
Virtex-UltraScale VCU110 Evaluation Pla	1.	xilinx.com	1.4	xcvu190-flgc210	2104	1.0	416	1074240
Virtex UltraScale+ VCU118 Evaluation P		xilinx.com	2.4	xcvu9p-flga2104	2104	2.0	832	1182240
Versal VCK190 Evaluation Platform		xilinx.com	2.2	xcvc1902-vsva21	2197	Rev B02	692	899840
Versal VMK180 Evaluation Platform		xilinx.com	2.2	xcvm1802-vsva2	2197	Rev B02	692	899840
Spartan-7 SP701 Evaluation Platform		xilinx.com	1.1	xc7s100fgga676-2	676	1.0	400	64000
								>

 $\times$ 

## Select "Microcontroller design preset" in the MicroBlaze Configuration selection

icroblaze Preset Con	figurations
Microcontroller	Suitable for running baremetal code
Real-time	Deterministic real-time processing on RTOS
Application	Embedded linux capable
Moncontroller Preset 32-bit Proces Programmable Logic	Tahin Docaled Load Memory sor Core Internat Controller Internat Controller Timer GPIO



## Review changes in the Project Summary and click "Finish"





### Windows Layout

The Microblaze design will load, and a Diagram window will appear on the right, where we can see all the IPs in the design including MicroBlaze IP, AXI Uartlite, AXI GPIO, and AXI Timer, which we will use to generate a PWM signal.



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### Connect "PWM" pin to external interface



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# Rename the external port "pwm0\_0" by changing the name under the "External Port Properties" to "SP701\_PWM"



	it rioperates	? _ O Ľ X
pwm0_0		←   →   Ø
Name:	VM_SP701	
Direction:	Output	
Net	⊐ axi_timer_0_pwm0	



# Select the wire between "pwm0" and "SP701\_PWM" by right clicking and selecting "Debug" to monitor the PWM of the Timer





## Use the Designer Assistance and select "Run Connection Automation", then click "OK"

This step will add System ILA to the design connected to the PWM



Modify the preset example design by creating a new wrapper, select "mb\_preset\_wrapper" under Design Sources in the Sources window





## Right-click on it and select "Remove file from the project"

Sources × Design Signals	В	oard ? _ D	5	Diagram × A
Q   ¥   ♦   +   छ   ● 0	0	<	>	Q Q 23
✓		Source Node Properties		Ctrl+E
✓ ● ∴ mb_preset_wrapper(	-	Open File		Alt+O
> mb_preset_i : mb		Replace File		
>  Constraints		Copy File Into Project		
> 🚍 Simulation Sources (1)		Copy All Files Into Project		Alt+1
> 😑 Utility Sources	×	Remove File from Project		Delete
		Enable File		Alt+Equals
		Disable File		Alt+Minus
		Move to Simulation Sources		
Hierarchy IP Sources Libr		Move to Design Sources		

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The "Remove Sources" window will appear and check the box for "Also delete the project local file/directory from the disk"





# Select "mb\_preset" design under the design sources window and Right-click then select "Create HDL Wrapper"

Sources × Design	Signals Board	? _ 0 6
Q	0 .	Updating O 🌣
✓	Source Node Propertie Open File	s Ctrl+E Alt+Cl
<ul> <li>Constraints</li> <li>Simulation So</li> <li>Utility Sources</li> </ul>	Generate Output Products	plate ucts
Hierarchy IP So	Replace File Copy File Into Project Copy All Files Into Proj	ect Alt+I



### Select "Let Vivado manage wrapper and auto-update"

### Create HDL Wrapper X You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file. Options Copy generated wrapper to allow user edits Let Vivado manage wrapper and auto-update ? OK Cancel

## In the Flow Navigator under Synthesis, click "Run Synthesis" and then Click "OK"

PROJECT MANAGER     Settings     Add Sources		
Language Templates		🝌 Launch Runs
후 IP Catalog		
P IP INTEGRATOR		Launch the selected synthesis or implementation runs.
Create Block Design		
Open Block Design		
Generate Block Design		Launch <u>d</u> irectory: Cefault Launch Directory>
SIMULATION	<ul> <li>SYNTHESIS</li> </ul>	Options
Run Simulation		Launch runs on local host: Number of jobs: 10 *
RTL ANALYSIS	Dun Sunthacia	
> Open Elaborated Design	Kun Synthesis	C Generate scripts only
SYNTHESIS		
Run Synthesis	> Open Synthesized Design	Don't show this dialog again
> Open Synthesized Design		? OK Cancel
IMPLEMENTATION		13
Run Implementation		
> Open Implemented Design		
PROGRAM AND DEBUG		
👫 Generate Bitstream		

> Open Hardware Manager

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## Connecting "PWM" signal to board interface

The SP701 Board includes 6 Pmods that we can use and assign the PWM signal to



## Connecting "PWM" signal to board interface

- 1. Go to Spartan-7 SP701 FPGA Evaluation Kit webpage
- 2. Under Resources download the SP701 Schematics
- 3. Open the xdc file and search for PMOD1\_PIN1
- 4. You'll find that it is connected to pin "C13"
- 5. In the next step we will assign PWM to pin C13



님 sp70	1_rev1	I.0_U1.xdc 🗵						
346	set_	property	PACKAGE_PIN	B22	[get_ports	"PMOD4_PIN7_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L9N_T1_DQS_16
347	set_	property	IOSTANDARD	LVCMOS33	[get_ports	"PMOD4_PIN7_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L9N_T1_DQS_16
348	set_	property	PACKAGE_PIN	B24	[get_ports	"PMOD4_PIN3_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L10P_T1_16
349	set_	_property	IOSTANDARD	LVCMOS33	[get_ports	"PMOD4_PIN3_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L10P_T1_16
350	set_	property	PACKAGE_PIN	C13	[get_ports	"PMOD1_PIN1_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L10N_T1_16
351	set_	property	IOSTANDARD	LVCMOS33	[get_ports	"PMOD1_PIN1_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L10N_T1_16
352	set_	property	PACKAGE_PIN	C14	[get_ports	"PMOD1_PIN8_R"]	;# Bank	16 VCCO - VCCO_3V3 - IO_L11P_T1_SRCC_16
353	set	property	IOSTANDARD	LVCMOS33	[get ports	"PMOD1 PIN8 R"]	;# Bank	16 VCCO - VCCO 3V3 - IO L11P T1 SRCC 16
								XILINX.

rdf0510-sp701-xdc.zip

# After the synthesis is completed that may take up to 10 mins click "Open synthesized design" to assign the PWM signal

Synthesis Completed



Synthesis successfully completed.

×

Next

Bun Implementation
 Open Synthesized Design
 View Reports

Don't show this dialog again





# Open the Scalar ports and assign "C13" to the "PWM signal" and change I/O Std to "LVCMOS33"

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## Rerun synthesis after the changes

	🝌 Launch Runs
	Launch the selected synthesis or implementation runs.
	Launch directory: Contract Con
✓ SYNTHESIS	Options
	● Launch runs on local host: Number of jobs: 10 ✓
Run Synthesis	Generate scripts only



> Open Hardware Manager

PROGRAM AND DEBUG
 Generate Bitstream

Flow Navigator

PROJECT MANAGER
 Settings
 Add Sources
 Language Templates

♀ IP Catalog

✓ IP INTEGRATOR

✓ SIMULATION

✓ RTL ANALYSIS

✓ SYNTHESIS

Run Synthesis

IMPLEMENTATION
 Run Implementation
 Open Implemented Design

Run Simulation

> Open Elaborated Design

> Open Synthesized Design

Create Block Design Open Block Design Generate Block Design Run implementation and generate a Bitstream by selecting "Generate Bitstream" under Program and Debug in the flow navigator

This bitstream generation may take up to 15 mins.





# **Export Design** select File $\rightarrow$ Export $\rightarrow$ Export Hardware in the Vivado Design Suite

~	Project				
	Add Sources Alt+A	EMENTED DESIGN - xc7s100fgga			
	<u>C</u> lose Project	rces Netlist × Properties			
	Close Implemented Design	ы			
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	Import +				
	Export	Export Hardware			
	Print Ctrl+P	Ext Constraints			
	Exit	Export Pblocks			
	Run Simulation	Export IBIS Model Exp <u>o</u> rt I/O Ports E <u>x</u> port Bitstream File			
<ul> <li>RTI</li> </ul>	ANALYSIS	Export Simulation			



### Click "Next" and select "Include Bitstream"

#### 🙏 Export Hardware Platform



#### Export Hardware Platform

This wizard will guide you through the export of a hardware platform for use in the Vitis or PetaLinux software tools.

To export a hardware platform, you will need to provide a name and location for the exported file and specify the platform properties.

🍌 Export Hardware Platform

#### Output

X

Set the platform properties to inform downstream tools of the intended use of the target platform's hardware design.

Pre-synthesis

This platform includes a hardware specification for downstream software tools.

#### Include bitstream

R

This platform includes the complete hardware implementation and bitstream, in addition to the hardware specification for software tools.

< Back

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Cancel

X

Cancel

### Under Tools $\rightarrow$ Select "Launch Vitis"

LOOIS	Kep <u>o</u> rts <u>w</u> indow Layout	view <u>r</u>
1	Eloorplanning	>
1	I/O Planning	Þ
	Iiming	*
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H :	Schematic	F4
	Show Connectivity	
1	S <u>h</u> ow Hierarchy	F6
1	Edit Device Properties	
	Create and Package New IP	
	Create Interface Definition	
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	Compile Simulation Libraries	
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## In Vitis IDE, go to File $\rightarrow$ New $\rightarrow$ Platform Project then click "Next"



## In the Platform window select "create a new platform from hardware (XSA)"

Select a platform from	n repository	Create a new j	platform from I	hardware (XSA) + Add O	Manage
Name	Board	Flow	Vendor	Path	
<					>
Platform Info					
General Info Name: Part:		cceleration Reso	ources	Domain Details Domains	^
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### Browse the XSA file and click "Next"

Select a	platform from repository 🗈 Create a new platform from hardware (XSA)		
Hardware	e Specification		
	Provide your XSA file or use a pre-built board description		
	vck190		
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XSA File	vmk180_es1	Browse	
raar e e enge	zc706	12	
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Platform	name:		
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# Set the project name to SP701\_MicroBlaze, then set the system project name to "your board name" system then click "Next"

Application project name: S	P701_MicroBlaze					
System Project						
Create a new system proje	ct for the application or sel	ect an existing one from the workpsace 0				
Select a system project  Create new	System project det	alls				
	Sustem project name: SP701 MicroBlate sustem					
	System project n	ame: SP701_MicroBlaze_system				
	Target processor					
	Select target proc	essor for the Application project.				
	Processor	Associated applications				
	microblaze_0	SP701_MicroBlaze				
	Show all process	ns in the hardware specification				

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## Click "Next" again to choose the Hello World template and press "Finish"

Vew Application Project	t	2	п х	Vew Application Project				×
Domain				Templates				•••
Select a domain for your p	roject or create a new domain			Select a template to create your proje	ect.			
Select the domain that the	application would link to or cr	eate a new domain		Available Templates:				
				Find:		Hello World		
Note: New domain created	d by this wizard will have all the	requirements of the application template selecte	ed in the	<ul> <li>Embedded software development</li> </ul>	templates	Let's say 'Hello World' in C.		
next step				Dhrystone				
Coloria damata	Denote details			Empty Application (C++)				
Select a domain	Domain details			Empty Application(C)				
+Create new		atom de la competitione de		Hello World				
	Name:	standalone_microblaze_0		IwIP Echo Server				
	Display Name:	standalone_microblaze_0		IwIP TCP Perf Client				
	Operating System:	standalone ~		IwIP TCP Perf Server				
	Processor	microblaze 0		IwIP UDP Perf Client				
	indecision.			IwIP UDP Perf Server				
	Architecture:	32-bit ~		mba_fs_boot				
				Memory Tests				
				Peripheral Tests				
				SREC Bootloader				
				SREC SPI Bootloader				
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0	< Back	Next > Finish	Cancel	(?)	< Back	Next > Finis	Cance	el
an Project		63				5		



## Build the hardware by right-clicking Platform $\rightarrow$ Build Project



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## Connect the board

Connect power cable to the board and connect a USB micro cable from the board's J5 USB JTAG connector to the Windows machine

Power the board using the power switch, which will automatically start the Built-in Self-Test



# Set up Tera Term for serial communication. Under set up, select serial port

○ T CP/IP	Host:	xilinx		
	Service:	<ul><li>☑ History</li><li>○ Telnet</li></ul>	TCP port#; 2	2
		SSH	SSH version: SSH	2 .
		○ Other	IP version: AUT	)
Serial	Port:	COM10: USE	3 Serial Port (COM10)	~



# Match the UART speed set in the Vivado UART IP setting for this project and save the new setting

Term: Serial port setup and co	nnection		×
Port:	COM10	New setti	ng
Speed:	115200	· · · · · · · · · · · · · · · · · · ·	
Data:	8 bit	Cancel	
Parity:	none	~	
Stop bits:	1 bit	~ Help	
Flow control:	none	$\sim$	
0	msec/char	0 msec/line	
Device Friendly Nar Device Instance ID: Device Manufacture Provider Name: FTE Driver Date: 8-16-20 Driver Version: 2.12	ne: USB Seria FTDIBUS\VIE er: FTDI )I 17 .28.0	al Port (COM10) )_0403+PID_6011+319311(	07268B



## Launch the hardware by selecting Run as $\rightarrow$ Launch Hardware (Single application Debug)



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### Hello World will appear on the serial communication in Tera Term

V Progress Information	— 🗆 X		
Programming FPGA			
55% 1MB 1.9MB/s ??:?? ETA			
	Cancel Details >>		
	COM10 - Tera Term VT	_	>
	File Edit Setup Control Window Help Hello World Successfully van Hello World application		
	Successfully ran nello world application		
	(c) Copyright 2021 Xiliny		

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## Pulse Width Modulation (PWM) application



## Under the Source folder in the Explorer window, rename the Hello-World.c to "PWM.c"

- SP701\_MicroBlaze\_system [ mb\_preset\_wrapper ]
  - SP701\_MicroBlaze [ standalone\_microblaze\_0 ]
    - Binaries
    - Includes
    - > 😕 Debug
    - Y 📑 SIC



┥ Rename Resource				$\times$
New name: pwm/c				
	Provine >	OK	Cancol	
	Preview >	UK	Cancel	



## Copy and Paste the PWM code to the C file

### > You can access the code under Demonstration steps in:

#### http://wiki.xilinx.com/Spartan-7+SP701+Evaluation+Kit+PWM+Tutorial

#### **Demonstration Steps**

The demonstration video will cover two quick examples of how to build a system from scratch. The first is a Hello World example using MicroBlaze and the second is the PWM application example.

#### Expand the following section to view the source code for the PWM demo

∨ PI	ease	copy the code below for the PWM application:
	1	# Copyright (c) 2021, Xilinx, Inc.
	2	# All rights reserved.
	3	<i>a</i>
	4	# Redistribution and use in source and binary forms, with or without
	5	# modification, are permitted provided that the following conditions are met:
	6	a
	7	# 1. Redistributions of source code must retain the above copyright notice,
	8	# this list of conditions and the following disclaimer.
	9	a
1	.0	# 2. Redistributions in binary form must reproduce the above copyright
1	1	# notice, this list of conditions and the following disclaimer in the
4	.2	# documentation and/or other materials provided with the distribution.
1	.3	4
1	.4	# 3. Neither the name of the copyright holder nor the names of its
1	.5	# contributors may be used to endorse or promote products derived from
1	.6	# this software without specific prior written permission.
1	7	4
	.8	# THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
	.9	# AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO,
	.0	# THE IMPLIED WARRANTES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR
	1	# PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR
1	2	I CONTRIBUTIONS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, CONTRIBUTIONS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL,
	3	# EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO,
1	4	PROCUREMENT OF SUBSITIUTE GOODS OK SERVICES; LOSS OF USE, DATA, OK PROFILS;     PROCUREMENT OF SUBSITIUTE CONTRACT, DATA ON PROFILE; STATEMENT CONTRACT, DATA ON PROFILE;     PROFILE;
1	5	WI UNE BUSINESS INTERKUPTION). NOWEVER CAUSED AND ON ANY THEORY OF LIABILITY,
	7	WITHERTER IN CONTRACT, STALL LABLETT, OR TORT (INCLOUING REGLETERCE OR OTHERTEC) ANTENNE THANK MAN VIT OF THE USE OF THREE CONTINUES EVEN TE
		<ul> <li>ONITERALSE/ ALISING IN ANT WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF</li> <li>ANUTER OF THE DOCESTRITY OF CICH DAMAGE</li> </ul>
	0	<ul> <li>Abvised of the possibility of such banade.</li> </ul>
	9	
	1	/* Include Header Files and Packaaes */
	2	#include <stdio.h></stdio.h>
3	3	#include "platform.h"
3	4	#include "xil printf.h"
3	5	#include "xtrctr.h"
3	6	
3	7	/* Device IDs Definition */
3	8	#define Gpioled XPAR_AXI_GPIO_0_DEVICE_ID
1	9	#define TWRCTR_ID XPAR_TWRCTR_0_DEVICE_ID
	0	HAFTAA HADTBacadddaace YDAD AYT HADTITTE A DACEADDD



## Right-click on the application project and select build





### Open Tera Term again and set up the serial communication Make sure that the board is connected

○ T CP/IP	Host:	xilinx			2
	Service:	<ul><li>☑ History</li><li>○ Telnet</li></ul>	TCP por	t#: 22	
		● SSH	SSH version:	SSH2	
		○ Other	IP version:	AUTO	
Serial	Port:	COM10: USE	3 Serial Port (CO	M10)	



# Right-click on the platform and select Run as $\rightarrow$ Launch Hardware to program the FPGA





### In Terminal, enter duty cycle





# In Vivado, to view the Integrated Logic Analyzer (ILA), select Hardware Manger then "Open target" and "Auto Connect"

#### PROGRAM AND DEBUG

- Generate Bitstream
- V Open Hardware Manager

Open Target

No hardware target is	s ope	n. Open target	
Hardware	ø	Auto Conn	
Q   ≚   ≑   Ø		Recent Targets  Available Targets on Server Open New Target	•



### 50% duty cycle waveform will be shown



## Change the duty cycle to 10%, refresh the waveform and run again the waveform will be updated

Duty Cycle is now: 50 Enter Duty Cycle in Bytes: Duty Cycle is now: 10 Enter Duty Cycle in Bytes:



### Apply the same steps for 90% duty cycle

Duty Cycle is now: 50 Enter Duty Cycle in Bytes: Duty Cycle is now: 10 Enter Duty Cycle in Bytes: Duty Cycle is now: 90 Enter Duty Cycle in Bytes:



## Conclusion

- In this tutorial:
  - We used Vivado example projects to built a customizable 32-bit embedded processor
  - Used Vivado IP Integrator to quickly add PWMIP block from IP library
  - Built the entire design without writing any RTL code
  - Used Vitis to validate operational Microcontroller by running Hello-World
  - Create and ran PWM code to change pulse-width of output signal
- PWMs are valuable in many designs as lighting, motor control, power supply control and much more
- Xilinx enables the ability to connect as many PWMs as I/Os are available
- This design can be used as a building block for you to start your own design

### **Available Resources**



Collateral

- <u>MicroBlaze Soft Processor Core</u>
   <u>Product Page</u>
- MicroBlaze Getting Started Wiki Page
- Spartan-7 Product Brief
- White Paper: Spartan-7 Family
- Cost Optimized FPGAs and SoCs
- > Unboxing SP701 FPGA Evaluation Kit
- MicroBlaze Quick Start Video



### **Tutorials & Guides**

- Quick Start Guide: MicroBlaze Soft
   Processor for Vitis 2021.1
- > MicroBlaze Processor Reference Guide
- Embedded Processor Hardware Design in Vivado Tutorial
- Creating and Packaging Custom IP in <u>Vivado</u>



### Workshops & Trainings

- No hardware experience? No problem! Xilinx MicroBlaze processors are for everyone.
- Arty-S7 Workshops:
- » Part 1: Learn about Xilinx FPGAs and Embedded Processing
- » Part 2: Building a Custom Microcontroller in <u>Minutes</u>
- » Part 3: Rapid Sensor Prototyping with Digilent Peripheral Modules
- Embedded System Design Training
- Sensor Fusion at the Edge with Spartan-7



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## **Thank You**

