



RFSoc Frequency Planner Quick Start Guide

Version 2.0
April 2022

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Revision History

Version	Date	Changes
1.0	Dec 22, 2021	Initial Release
2.0	April 20, 2022	Enabled DAC power measurement to show 5 digits
		Fixed sampling rate tooltip content
		Increased DPD 5th order and 7th order by 5dB
		Added PLL simulation tab
		Fixed DAC DUC bypassed mode HD2/HD3 location
		Added filter response overlay to all blocks with filtering
		Added additional tooltips to most fields and blocks
		Changed ADC DSA and RF power input relationship
		Added external PLL requirement warning for DAC Fs outside internal PLL range
		Enhanced data saturation error messaging and Fs outside device range warning
		Added 'real/cplx' indicator to each of the DAC and ADC stages
		Changed usage notes to quick start guide pdf

Overview

- ▶ The RFSoc Frequency Planner is made available by AMD for RFSoc device users to simulate high-level behavior of the RF Data Converters to assist in choosing a suitable frequency plan and device configuration for the target use case.
- ▶ It does not model the analog performance of the data converters; the performance metrics such as HD2/3, NSD, etc., are intended to be inputs from the user. Defaults values are provided for ease of getting started.
- ▶ Only impairments that are typically applicable to frequency planning is included.
- ▶ It is not intended to reflect or guarantee precise RF performance of the Data Converters. For specific device specification please refer to the datasheet and associated documentation for the device at www.xilinx.com.
- ▶ The simulated result is an approximate prediction of the data converter behavior; this in turn allows the user to run through various configuration scenarios quickly.
- ▶ It's highly recommended that the user validate the configuration of choice with the actual hardware. This can be carried out with the various RFSoc evaluation boards offered by AMD Xilinx.
- ▶ The three main features of the Frequency Planner are
 - to visualize location of signals and impairments of the data converters in the time and frequency domain for optimal selection of sampling rate and operating band placement.
 - to examine the signal level and characteristics of each sub-block of the data converter tile for proper signal scaling in the system.
 - to estimate the internal PLL phase noise performance with a given phase noise performance of the reference oscillator input.

General Assumptions, Conventions, and Limitations

- ▶ All digital filters in the DAC and ADC digital processing blocks use the same filter coefficients as in the actual hardware; the blocks include:
 - For DAC: P/Q Resampler, DUC Interpolation, Image Reject Filter, and Inverse Sinc.
 - For ADC: DDC Decimation, and P/Q Resampler.
- ▶ Signal level units are always in dBFS (dB full scale) for digital signal and dBm for analog RF signal.
 - For DAC: All blocks are in dBFS except for the DAC output, which is in dBm.
 - For the ADC: All blocks are in dBFS except for the ADC input, which is in dBm.
 - See [Signal Power Calculations](#) slide for detail calculation methods.
- ▶ Signal source for ADC and DAC are generated with bandlimited AWGN except for CW tones.
 - Band limited signals are not standards specific; they are generated with random data for each run / update.
 - BW (bandwidth) should be set to 0 for CW (continuous wave) tones.
 - The minimum supported signal bandwidth is 5MHz, maximum bandwidth is 85% of input Nyquist bandwidth. Small signal bandwidth will require longer run time. Smaller RBW for the spectrum plot (resolution bandwidth) will also lengthen the run time.
- ▶ Computer Monitor with 1080P resolution or better is recommended for best user experience.
- ▶ PLL phase noise simulation result is for typical value only. Result over PVT will be in a banded range. Consult your local AMD Xilinx FAE for PVT characterization report of internal PLL performance.

General Assumptions, Conventions, and Limitations

- ▶ All sampling rates and frequency units are in Msps or MHz unless otherwise noted.
- ▶ DAC output only supports frequency domain and CCDF plot, time plot is not applicable. Use the Inverse Sinc stage output to view the time plot instead.
- ▶ CCDF of the DAC RF output is computed on the complex RF envelope of the signal, which has a 3dB PAR reduction from the real digital signal from the Inverse Sinc stage prior.
- ▶ Power measurement is only valid for the DAC output stage under the DAC panel. It's valid for all stages under the ADC panel.
- ▶ NSD is always added to the signal, regardless of the Enable status; however, the value can be changed.

Signal Power Calculations

▶ dBFS (dB Full Scale) convention for DAC

- Both RMS (root mean squared) and peak power are calculated for each digital block outputs X_{out} , and always referenced to a full scaled complex CW. The formula used is as follows.

- $Power_{rms}(dBFS) = 20 * \log_{10} \left(rms \left(\frac{X_{out}}{2^{15}} \right) \right)$

- $Power_{peak}(dBFS) = 20 * \log_{10} \left(\max(abs(\frac{X_{out}}{2^{15}})) \right)$

- A complex CW $X_{out}(N) = 2^{15} * e^{2 * \pi * i * \frac{f_c}{f_s} * N}$ has $Power_{rms} = 0dBFS$ and $Power_{peak} = 0dBFS$
- A real CW $X_{out}(N) = 2^{15} * \cosine \left(2 * \pi * \frac{f_c}{f_s} * N \right)$ has $Power_{rms} = -3dBFS$ and $Power_{peak} = 0dBFS$

▶ dBFS (dB Full Scale) convention for ADC

- Keeping with ADC full scale convention, blocks with real output (i.e., ADC Core, QMC), full scale is referenced to a full scaled real CW signal and calculated as follows.

- $Power_{rms}(dBFS) = 20 * \log_{10} \left(rms \left(\frac{X_{out}}{2^{15} * \sqrt{0.5}} \right) \right)$

- $Power_{peak}(dBFS) = 20 * \log_{10} \left(\max(abs(\frac{X_{out}}{2^{15} * \sqrt{0.5}})) \right)$

- A real CW $X_{out}(N) = 2^{15} * \cosine \left(2 * \pi * \frac{f_c}{f_s} * N \right)$ has $Power_{rms} = 0dBFS$ and $Power_{peak} = +3dBFS$
- Note that the Peak power of a CW has positive dBFS value (+3dBFS) due to this convention
- Digital blocks with complex output (i.e., Mixer, DDC, etc.), the calculation for power in dBFS is the same as that for the DAC.
- A complex CW $X_{out}(N) = 2^{15} * e^{2 * \pi * i * \frac{f_c}{f_s} * N}$ has $Power_{rms} = 0dBFS$ and $Power_{peak} = 0dBFS$
- A real CW $X_{out}(N) = 2^{15} * \cosine \left(2 * \pi * \frac{f_c}{f_s} * N \right)$ has $Power_{rms} = -3dBFS$ and $Power_{peak} = 0dBFS$

Quick Start for each panel

GUI Overview

The screenshot shows the RFSoc Frequency Planner GUI with the following annotated components:

- Tab selection for converter type or PLL:** Points to the DAC, ADC, and PLL tabs at the top.
- Blocks available in RFSoc DFE:** Points to the DAC block configuration area.
- Input signal source, up to 4 component carriers, not part of the hard IP:** Points to the input frequency and power settings.
- Click to Start or Update Simulation:** Points to the UPDATE DAC button.
- Status and error message:** Points to the status bar at the top right.
- Channel power measurement:** Points to the power measurement table.
- RMS and Peak power stats for each block output:** Points to the power statistics for the DAC Core.
- Block for each stage of the hardened data converter tile:** Points to the DAC Core block.
- Plot trace on/off viewing option:** Points to the legend for the DAC Output Spectrum plot.
- Frequency domain plot of stage/block output, click on stage to select its output to be displayed:** Points to the DAC Output Spectrum plot.
- RFSoc family and device selection:** Points to the RFSoc Family and Device PN dropdowns.
- Device info, read only:** Points to the Device Info table.
- Device impairments, default values for reference only, user should change the values to better reflect what's being used:** Points to the Impairments table.
- Time domain plot or Peak to Average (PAR) distribution plot:** Points to the CCDF plot.

DAC Simulation Quick Start

1. Select RFSoc Device of choice:

RFSoc Family: RFSoc DFE
Device PN: ZU67DR

2. Edit or confirm existing impairment values for the DAC column.

Spec	DAC	ADC	Enable
NSD[dBm/Hz]	-165	-152	<input checked="" type="checkbox"/>
HD2[dBc]	-65	-65	<input checked="" type="checkbox"/>
HD3[dBc]	-70	-70	<input checked="" type="checkbox"/>
TIS[dBc]	NaN	-85	<input checked="" type="checkbox"/>
OIS[dBFS]	NaN	-85	<input checked="" type="checkbox"/>

3. Enter Input data sampling rate and desired RMS power level.

- Select DUC enable/disable option; input Sampling rate is the same as DAC sampling rate for DUC bypassed
- Modulated signal typically has 10 to 12dB PAR (peak to average ratio); single CW tone has 0dB PAR.

Input Fs Msps: 491.52
Rms Pwr dBFS: -15
DUC Enable:

4. Configure the baseband input signal in the signal composition table

- Supports up to 4 component carriers (CC); at least one CC must be enabled.
- Enter carrier frequency Fc in MHz, signal bandwidth in MHz (0 for CW), and relative power in dB for each CC.
- Baseband composite signal total instantaneous bandwidth should be < Nyquist BW (Fs for cplx, Fs/2 for real).

CC Fc (MHz)	BW (MHz)	CC Pwr (dB)	Enable	
0	100	0	<input checked="" type="checkbox"/>	CC0
75	50	-3	<input type="checkbox"/>	CC1
-75	50	-3	<input type="checkbox"/>	CC2
150	100	0	<input type="checkbox"/>	CC3

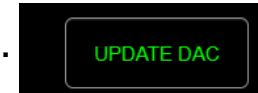
5. Configure each of the DAC stages with the desired setting (see PG269 for details of each stage)

- If RFSoc DFE device is selected, CFR, P/Q, and DPD blocks are enabled for use
 - The CFR block and DPD block used here are not the same as the AMD Xilinx IP. They are very simple models provided to enable signal power level and frequency spectrum planning only. See tooltips for more info.
 - The CFR block allows the user to reduce the PAR of the signal by specifying a target PAR value. Not all target values are achievable due to the simplicity of the model. Best effort is used.
 - The DPD block simulates signal expansion in the time and frequency domain of a typical DPD function. It simply adds IMD3 and IMD5 to the signal; level of the IMD's in dBc can be adjusted by the user to fine tune the amount of spectrum expansion from the DPD. Note that the PAR of the output signal will generally increase to resemble that of a Gaussian bandlimited signal; user cannot predefine the exact output PAR value.
 - Both blocks have adjustable output gain for further fine tuning the signal level at each of the stages.

DAC Simulation Quick Start

6. Ensure that all stages have valid sampling rate for the chosen device after configuration change. Invalid sampling rates will be shown in red. It is possible to run the simulation with invalid sampling rates, but not recommended.

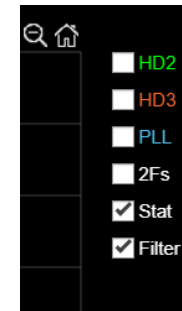
7. Press 'UPDATE DAC' to start/update simulation with the selected configuration.



8. Check 'Status' bar for any error or warning messages.

9. Simulation output is now updated on the 2 plots; below are some options after the update is done.

- Select or deselect each of the trace options next to the Output Spectrum plot to view location and signal level of each of the impairments.
- Click on any of the stages to view the output of the stage
- Check 'Stat' to view RMS and Peak power at the output of each stage (see snippet on right)
- Check 'Filter' to view the filtering response of an applicable filter stage (see snippet on right)
- Configure the Power Measurement and Click on the box to measure channel power for the DAC output
- Go to File → Save Configuration to save a copy of the current configuration. The DAC, ADC, and PLL will all be saved.



ADC Simulation Quick Start

1. Select RFSoc Device of choice:

RFSoc Family	RFSoc DFE
Device PN	ZU67DR

2. Edit or confirm existing impairment values for the ADC column.

Spec	DAC	ADC	Enable
NSD[dBm/Hz]	-165	-152	<input checked="" type="checkbox"/>
HD2[dBc]	-65	-65	<input checked="" type="checkbox"/>
HD3[dBc]	-70	-70	<input checked="" type="checkbox"/>
TIS[dBc]	NaN	-85	<input checked="" type="checkbox"/>
OIS[dBFS]	NaN	-85	<input checked="" type="checkbox"/>

3. Enter Input Sampling rate of the ADC and desired RMS power level at ADC Core output.

- Select fast (Dual) or slow (Quad) ADC if device has both types; select DDC enable/disable option.

ADC Fsamp Msps	2949.12	DDC Enable
Rms Pwr dBFS	-12	Quad ADC

4. Configure the RF input signal in the signal configurator table

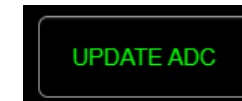
- Supports up to 4 component carriers (CC); at least one CC must be enabled
- For valid ADC support use case, only carriers in the same Nyquist zone should be enabled.
- Enter RF carrier frequency Fc in MHz, signal bandwidth in MHz (0 for CW), and relative power in dB for each CC.
- Composite signal total instantaneous bandwidth should be < Nyquist BW (Fs for cplx, Fs/2 for real).

CC Fc (MHz)	BW (MHz)	CC Pwr (dB)	Enable	
3800	100	0	<input checked="" type="checkbox"/>	CC0
3500	100	0	<input type="checkbox"/>	CC1
1900	20	0	<input type="checkbox"/>	CC2
4900	50	0	<input type="checkbox"/>	CC3

5. Configure each of the ADC stages with the desired setting (see PG269 for details of each stage)

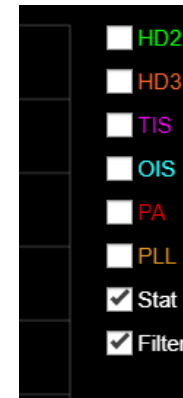
6. Ensure that all stages have valid sampling rate for the chosen device after configuration change. Invalid sampling rates will be shown in red. It is possible to run the simulation with invalid sampling rates, but not recommended.

7. Press 'UPDATE ADC' to start/update simulation with the selected configuration.



ADC Simulation Quick Start

8. Check 'Status' bar for any error or warning messages
9. Simulation output is now updated on the 2 plots; below are some options after the update is done.
 - Select or deselect each of the trace options next to the Output Spectrum plot to view location and signal level of each of the impairments.
 - Click on any of the stages to view the output of the stage
 - Check 'Stat' to view RMS and Peak power at the output of each stage (see snippet on right)
 - Check 'Filter' to view the filtering response of an applicable filter stage (see snippet on right)
 - Configure the Power Measurement and Click on the box to measure channel power for any of current active ADC stage
 - Go to File → Save Configuration to save a copy of the current configuration. The DAC, ADC, and PLL will all be saved.



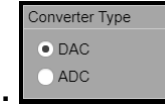
PLL Simulation Quick Start

1. Select RFSoc Device of choice:



RFSoc Family: RFSoc DFE
Device PN: ZU67DR

2. Click on PLL Panel then select Converter Type (ADC and DAC PLL settings are slightly different).



Converter Type
 DAC
 ADC

3. Enter desired converter sampling rate and RF frequency at which the phase noise is evaluated.



Sampling Rate	9830.4
RF Carrier Freq	1000

1. Note that AMD Xilinx datasheet and characterization report of internal PLL defaults RF Carrier Frequency to 1000MHz, unless otherwise noted.

4. Enter input reference oscillator frequency, and its phase noise at the different offsets.

5. Enter R divider value, incorrect entry will be auto changed to a valid one. Typically value of 1 is used. See datasheet DS926 for valid range.

6. Press 'UPDATE PLL' to start/update simulation with the selected configuration.



7. Check for 'Status' bar for any error or warning messages.

8. Simulation output is now updated on the main plot. 4 traces are plotted to show the various noise contributions.

- PLL PN – this is the noise from the phase locked loop (including PFD, charge pump, dividers, 1/f flicker, loop filter).
- Ref Osc PN - this is the noise contributed from the input reference oscillator
- VCO PN – this is the noise contributed from the VCO
- Total PN – this is the final output phase noise of the PLL output, scaled to the desired RF frequency (default is 1GHz)
- The total PN result is also tabulated at various common offsets in the table on the right.
- The results in the table can also be copied to the PLL impairment table for ADC and DAC simulation use.



RF Out Phase Noise	
100Hz	-103.66
1kHz	-112.86
10kHz	-120.22
100kHz	-126.94
1MHz	-132.16
10MHz	-149.69
100MHz	-161.75

Copy to Impairment Table

Other Usage Notes and Tips

- Configurations can be saved, loaded, and shared.
- Configuration files are only backward compatible for minor revisions of the tool, for instance
 - Version 2.0 and 2.x configuration files are compatible with each other.
 - Version 1.0 and 2.0 configuration files are not compatible with each other.
- Software versions are installed in difference folders, thus older version will not be overwritten.
 - More than 1 instance of the software can be running concurrently, for same version or difference versions.
- Software Help is generally done with tooltips; hover mouse over block to view
- Any changes to the ADC/DAC configuration and RBW (resolution bandwidth of power spectrum plot) requires an 'Update' to get new results.
 - Changes to other plot options do not need a new 'Update', simply click on the stage of interest to view the changes in plot option selection.
- Trace of the various digital filters are scaled to the signal level for ease of viewing, it does not represent the actual gain of the filter.
- The NCO Frequency value for the Mixers (ADC and DAC) does not use the same convention as that in the RFSoc API, this is done for ease of use. Below is the equation used for the mixer. See tooltip for more detail.
 - $$X_{out}(N) = X_{in}(N) * \exp(2 * \pi i * i * \frac{F_{NCO}}{F_{samp}} * N)$$
- Some values outside the specification of the selected device may be allowed for simulation to run for the purpose of hypotheticals. Invalid values will still be flagged. User should be cautious on what's realizable with the device.

Other Usage Notes and Tips

- Both DAC and ADC simulation supports up to 4 CC's (component carriers), some use cases include
 - Two CW tones, one at each edge of the desired band. This can be used to check some of the filtering artifacts and alias.
 - One wanted modulated signal and one high level CW. This can be used to examine the receiver blocker situation.
 - 2 different signal on either side of DC. This can be used to visualize spectral inversion at different stages of the signal chain.
 - Signals from different RF bands into the ADC to see how the alias of one band affects another; useful for co-location deployments.
- On the DAC panel, CFR, P/Q, and DPD blocks are always bypassed if 'DUC Bypass' Datapath is selected. This is only applicable to RFSoc DFE device. Other devices do not have these blocks.
- Click 'Restore default' for any of the panels in case the tool is stuck in some unknown / invalid configuration; then begin changing the configuration to the one desired.
- NSD, HD2, HD3, TIS, and OIS levels can be changed to make the plots and traces visually stand out for ease of identification, and experiment with hypotheticals.
 - Example, setting the ADC NSD to -174 will prevent the noise floor from masking the location of the HD2 and HD3 components of the ADC. This is especially usefully for bandlimited signals.

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