2021 Xilinx Security Working Group (XSWG) North America

Day 1

Monday, November 8, 2021	
All times in Mountain Time Zone (MDT)	
Topic	**Time**
Welcome and Introductions	8:00am - 8:15
Versal Security Features	8:15 - 9:30
Break	9:30 - 9:45
Versal Asymmetric HWRoT Secure Boot	9:45 - 10:40
Versal Symmetric HWRoT Secure Boot	10:40 - 11:40
Lunch	11:40 - 12:50pm
Versal External Secure Storage	12:50 - 1:20
Versal Isolation/Access Controls	1:20 - 2:00
Break	2:00 - 2:15
Versal Glitch Detector Characterization	2:15 - 3:00
Versal Secure HW Characterization	3:00 - 3:45

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Day 2

Tuesday, November 9, 2021	
All times in Mountain Time Zone (MDT)	
Topic	**Time**
Versal Readiness and Roadmap	8:00am - 8:30
Versal AHWRoT Lab Demo	8:30 - 9:20
Break	9:20 - 9:35
Versal SHWRoT Lab Demo	9:35 - 10:35
Versal Authenticated JTAG Lab Demo	10:35 - 11:20
Lunch	11:20 - 12:30pm
Versal eFUSE-Enabled Fault Mitigation Features Lab Demo	12:30 - 1:05
Zynq UltraScale+	1:05 - 1:55
Break	1:55 - 2:10
Future Products Roadmap	2:10 - 3:05

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Day 3

Wednesday, November 10, 2021	
All times in Mountain Time Zone (MDT)	
Topic	**Time**
Attacking Semiconductor Devices	8:00am - 8:55
Supply Chain Security	8:55 - 9:55
Break	9:55 - 10:10
Automotive Security (ISO21434 and J3101)	10:10 - 10:55
Zynq UltraScale+ HSM IP	10:55 - 11:35
Lunch	11:35 - 12:45pm
Kria SOMs : Building a More Secure System On a Module	12:45 - 1:30
DataCenter Security	1:30 - 2:30
Break	2:30 - 2:45
Guidance on Essential Security Resources / Information	2:45 - 3:35
Wrap Up	3:35 - 3:50