< b<>com conversion IP>

/<User Guide>/

< SDR to HDR>

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< **Diffusion** >
Public

< **Auteur** >
Benoît LE LUDEC

Revision history

Version	Date	Description of the modifications
1.0	07/12/2020	Initial release

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1 INTRODUCTION

1.1 System Description

Hardware acceleration allows for faster tone mapping conversion with the same quality and a better bitrate than converting with only software.

The system on which the hardware accelerator is running is shown in the following figures.

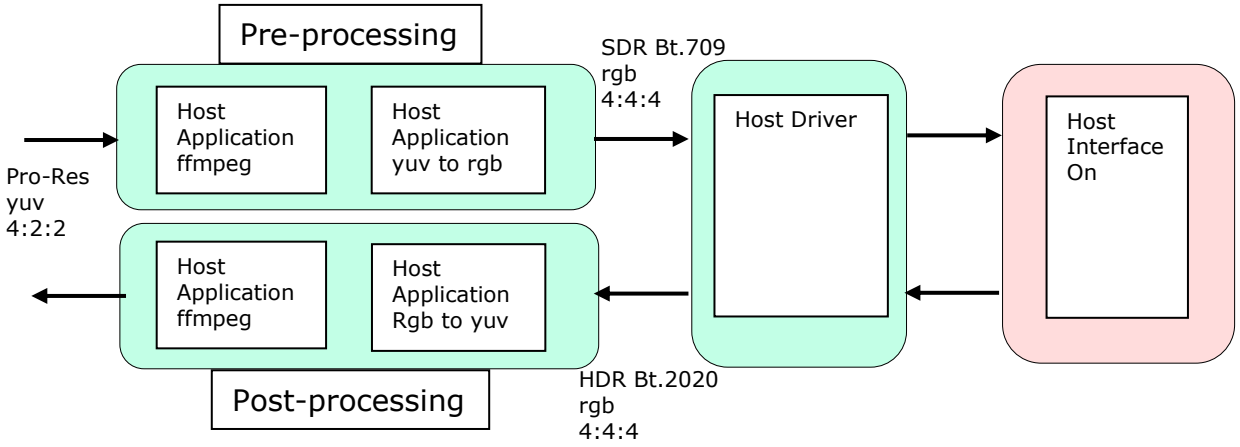

Figure 1: Software configuration

The conversion IP is implemented in the FPGA that is located on the PCI-e card.

In the pre-processing, the application ffmpeg allows the yuv video sequence in format Pro-Res yuv 4:2:2 to be converted to the format yuv r210. The application yuv-to-rgb allows to convert yuv to rgb with the colorspace matrix required for this conversion.

In the post-processing, the operations are the mirror of the pre-processing.

1.2 Tone expansion Throughput

The tone expansion is completely self-adaptative to the video content and no metadata are used to perform the conversion. The HDR Bt.2020 output can be select among Perceptual Quantizer (PQ) law, Hybrid Log Gamma (HLG) and Slog3.

Through a generic parameter, the FPGA can contain several instances of the IP to process several pixels of the same stream simultaneously.

The conversion process is independent from the resolution and it can operate from 1920x1080 @60p up to 4k@60p

2 TONE MAPPING PARAMETERS

2.1 Basic parameters of the IP

- Pixel format: progressive rgb 4:4:4
- Resolution: 1080p, 4k
- Frames per second: the maximum supported fps varies based on resolution. Maximum input bandwidth should not be exceeded.
- Bitrate: the bit-rate for the FPGA processing is dependant from the clock and the number of pixels processed at the same time.

2.2 Interfaces

- Input video:
    - Progressive video formats up to UHD
    - Compliant to BT.709
- Output video:
    - Same video format than input
    - Compliant to BT.2100 (PQ, HLG)
    - Compliant to BT.2020 and S-log3
- Protocol
    - Compliant to AXI-4 streaming video protocol

› IP input/output sampling:

- RGB 4:4:4 on 10 bits

- Number of IP instances: up to 8

3 DIGITAL RIGHTS MANAGEMENT

3.1 Subscribe and Run DRM

The IP conversion usage is protected and monitored through digital rights management (DRM) provided by Accelize. The DRM IP is part of the sdr2hdr converter binary running on the FPGA.

Use the following steps to subscribe and run:

(1) Create an account on the Xilinx App Store (https://appstore.xilinx.com)

(2) Subscribe to the SDR2HDR converter

(3) Generate and save an access key (cred.json) if not already done during the subscription process

(4) Run the converter

4 LIMITATIONS

1- Output: only PQ is supported on this application

2- Resolution: 1920x1080

3- Video sequence format: Pro-Res yuv 4:2:2

4- Number of instances: fixed to 4 pixels processed simultaneously

5- Number of streams: 1 stream can be processed

6- Bit-rate: the bit-rate of the complete processing is very dependant from the pre-post processing that are not optimized.

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