Spartan®-6 FPGA Migration Journey Webinar Q&A

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1. Is there an EOL to the Spartan-6 FPGA?

   No, Spartan®-6 devices are not End-of-Life. The Spartan-6 FPGA is under supply constraint—we currently have significantly more demand than our fab can supply.

2. Is the availability of Artix-7 FPGAs better than Spartan-6 FPGAs?

   Artix®-7 FPGAs and all newer devices have much better supply chain availability than the Spartan-6 FPGA.

3. Are Spartan-7 FPGAs offered in TQFP packaging?

   Unfortunately, no. TQFP packages do not meet performance and signal integrity requirements of Spartan-7 FPGAs.

4. Are there any "prototype supplies" available?

   Please work with your salesperson. We are making prototype quantities available for certain devices. This must be escalated through your sales team.

5. Are there plans for Spartan-7 devices with better I/O-to-logic ratios?

   Spartan-6 devices do indeed offer excellent I/O-to-logic ratios. However, as technology nodes shrink, the cost of I/O goes up, not down like most other IP blocks. For Spartan-7 devices, I/O-to-logic-cell ratio is on par with Spartan-6 devices for most densities, however, there are some outliers.

6. Is there a PCB design checklist for Spartan-7 devices?

   View UG483 for a comprehensive schematic review checklist that complements this user guide.

7. Which of the 7 series parts are offered with a leaded BGA option?

   Any part can be made with leaded balls. Please work with your salesperson.

8. When can we expect the stabilization of 7 series lead times?

   This is an industry-wide problem, and unfortunately, no one has this answer. However, we project to have a better supply next year.

9. What is the difference between MCB from Spartan-6 to Spartan-7 FPGA?

   The Spartan-7 FPGA’s soft memory controller block (MCB) has much more flexibility than the hard MCB in Spartan-6 devices.

10. Is the Vitis tool layer built on top of Vivado ML tools, and a tool that replaces SDK?

    Yes, Vivado® ML tools offer a hardware-centric approach to designing hardware, while Vitis™ tools offer a software-centric approach to developing *both* hardware and software.

11. Why are CDC problems resolved more effectively with Vivado ML tools and newer families?

    The improved handling of clock domain crossings (CDCs) is partly due to the newer device architectures, but it's mostly because Vivado ML is a timing driven tool—in contrast to the ISE® tool, which is a basic routing and mapping tool. Vivado ML is clock aware and diagnoses all clocks before doing any placement or routing.

    Vivado ML offers better clock domain crossing analysis with the CDC report and the clock interaction report.

12. Any pitfalls to avoid when converting from ISE CoreGenerator IP to newer versions in Vivado ML?

    Keep the following in mind when porting IP from ISE to Vivado tools:

    - Make sure you get the AXI interfaces right. The AXI Reference Guide (UG1037) offers a few simple guidelines to make this easier.
    - Vivado ML gives you most of the IP you'll need.
    - Double-check your constraints to make sure they're correct.
    - Clock domains are slightly different in Vivado ML, namely where Vivado ML starts "clock 0". This is explained in the Migrating Spartan-6 Designs to 7 Series & Beyond white paper.

13. Can I find migration resources in one place?

    Yes. visit the migration hub at: https://www.xilinx.com/products/silicon-devices/fpga/spartan-6.html#migrationResources

14. How much logic is consumed by the soft IP memory controller?

    Logic utilization can be found in product guide UG586.