Partial Reconfiguration AXI Shutdown Manager v1.0

LogiCORE IP Product Guide

Vivado Design Suite

pg305 (v1.0) April 4, 2018

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Chapter 1

IP Facts

The Xilinx Partial Reconfiguration AXI Shutdown Manager safely handles AXI4MM and AXI4-Lite interfaces on a Reconfigurable Partition when it is undergoing partial reconfiguration (PR), preventing system deadlock that can occur if AXI transactions are interrupted by PR.

Features

- AXI4MM and AXI4-Lite support
- Optional Signal based or AXI4-Lite control
- Optional AXI4-Lite status (signal status is always available)
- Optional termination control

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+™, UltraScale™, 7 series
Supported User Interfaces	AXI4-Lite
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	XDC
Simulation Model	Source HDL
Supported S/W Driver[2]	None
Tested Design Flows[3]	
Design Entry	Vivado Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.

LogiCORE IP Facts Table	
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx® at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. Standalone driver details can be found in the software development kit (SDK) directory (<install_directory>/SDK/<release>/data/embeddedsw/doc/xilinx_drivers.htm). Linux OS and driver support information is available from the Xilinx Wiki page.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Chapter 2

Overview

One or more Partial Reconfiguration AXI Shutdown Managers can be used to make the AXI interfaces between a Reconfigurable Partition and the static logic safe during Partial Reconfiguration (PR). When active, AXI transactions sent to the Reconfigurable Module (RM), and AXI transactions emanating from the Reconfigurable Module, are terminated by the core because the Reconfigurable Module might not be able to complete them. Failure to complete could cause system deadlock.

When inactive (In Pass Through mode), transactions are passed unaltered.

Feature Summary

Multiple Options for Status and Control

The Partial Reconfiguration AXI Shutdown Manager can be controlled and queried using single signals or an AXI4-Lite interface.

Partial Reconfiguration Controller Interoperability

The Partial Reconfiguration AXI Shutdown Manager connects directly to the Partial Reconfiguration Controller using the signal based control interface.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx® Vivado® under the terms of the Xilinx End User License.

For more information about this core, visit the PR AXI Shutdown Manager product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Introduction to Shutdown

Designers of Partially Reconfigurable systems must ensure that there are no AXI transactions in-flight at a Reconfigurable Module's interfaces when it is removed from a system, and that no transactions are sent to a Reconfigurable Partition that has no active RM. Failure to ensure this can lead to system deadlock.

For example, if an AXI master in the static requests a 256 word read from a Reconfigurable Module, and the RM is removed before supplying all of the data, that master may hang indefinitely. Alternatively, the RM might have launched a 256 word write transaction and been removed before it could supply all the data. The attached slave might hang waiting on the rest of the data, which will no longer be sent.

If the design cannot ensure through normal operation (for example, in the software stack) that all AXI Transactions will be completed, then the AXI Shutdown Manager IP can be used.

Operation

Modes of Operation

The IP works in two modes - Pass Through and Shutdown.

- In Pass Through mode, the core is functionally transparent but adds some latency to the AXI transactions. Transactions from the upstream master are received on the slave side of the core, passed to the master side of the core, and sent to the downstream slave. Responses from the downstream slave are received on the master side of the core, passed to the slave side of the core, and sent to the upstream master.
- In Shutdown mode, transactions that are received on the master side of the core are handled by the Shutdown Manager based on a configuration option. They are either terminated by the Shutdown Manager, or held until the mode is switched back to Pass Through mode. See Responding to Transactions in Shutdown Mode for more information.

Changing the Mode of Operation

The IP changes mode when requested and all the previously accepted transactions have been resolved. Each AXI channel contains a small FIFO, so 16 transactions can be outstanding. A mode change can be requested using the `request_shutdown` signal, or the `request_shutdown` register bit, depending on which is enabled.

All AXI transactions are stored with the value of `request_shutdown` that existed when the transaction was received. For example, if a transaction is received when `request_shutdown` is asserted, it is stored as a transaction that is to be handled by the Shutdown Manager IP. Deasserting `request_shutdown` before the transaction is processed will not change how it is handled by the core. The reverse is also true. A transaction received when `request_shutdown` is deasserted will be handled as such regardless of the value of `request_shutdown` when the transaction is processed.

Control Status

The Shutdown Manager IP provides a signal interface and an AXI Lite register interface to control the core. Only one of these can be enabled at a time. It also provides signal and AXI Lite register access to the core's status. The AXI Lite interface is optional, but the status signals are always present. They can be left unconnected if not required.

Integration with PRC

The Shutdown Manager IP has been designed to operate with the Partial Reconfiguration Controller IP. The `vsm_<name>_rm_shutdown_req` output of the appropriate Virtual Socket Manager can be connected directly to the Shutdown Manager's `request_shutdown` control signal. If multiple Shutdown Managers are used, the `vsm_<name>_rm_shutdown_req` signal can be connected to each's `request_shutdown` control signal directly. See *Partial Reconfiguration Controller* (PG193) for more information.

Performance

For full details about performance and resource use, visit the Performance and Resource Use web page.

Resource Use

For full details about performance and resource use, visit the Performance and Resource Use web page.

Port Descriptions

Port Names

Table 1: **Port Descriptions**

Port Name	I/O	Description
clk	I	Clock
reset/resetn	I	Reset. Active High/Low depending on core configuration
s_axi_ctrl_*	I, O	AXI4-Lite register interface[1]
request_shutdown	I	Assert to request entry to Shutdown Mode. Deassert to request entry to Pass Through mode
shutdown_requested	O	Asserted when shutdown has been requested, either by the `request_shutdown` signal, or through the register interface. This signal can be used to drive the `request_shutdown` input of other Shutdown Manager instances
in_shutdown	O	Asserted when shutdown has been requested and all pending transactions have been handled. This signal signifies that both the Read Channel and the Write Channel have entered Shutdown Mode
wr_in_shutdown	O	Write Channel In Shutdown. Asserted when shutdown has been requested and all pending write transactions have been handled. This signal signifies that the Write Channel has entered Shutdown Mode
rd_in_shutdown	O	Read Channel In Shutdown. Asserted when shutdown has been requested and all pending read transactions have been handled. This signal signifies that the Read Channel has entered Shutdown Mode
wr_irq	O	A level-based interrupt that is asserted for a clock cycle when a write transaction is received and `request_shutdown` is asserted. This transaction will not be passed on by the core[2], and the interrupt is to alert the system that something is trying to communicate with a Reconfigurable Module that is no longer present.
rd_irq	O	A level-based interrupt that is asserted for a clock cycle when a read transaction is received and `request_shutdown` is asserted. This transaction will not be passed on by the core[2], and the interrupt is to alert the system that something is trying to communicate with a Reconfigurable Module that is no longer present.
irq	O	A level-based interrupt that is asserted when either `wr_irq` or `rd_irq` is asserted
s_axi_*	O	The AXI[1] slave interface that the upstream master attaches to

Table 1: **Port Descriptions** *(cont'd)*

Port Name	I/O	Description
m_axi_*	I, O	The AXI[1] master interface that the downstream slave attaches to

Notes:

1. For a description of AXI4, AXI4-Lite and AXI Stream signals, see the *Vivado Design Suite AXI Reference Guide* (UG1037).
2. If the core is configured to use back-pressure (see Responding to Transactions in Shutdown Mode), then the transaction will be passed on to the downstream slave once the core has exited Shutdown Mode

Register Space

The following table describes the Partial Reconfiguration AXI Shutdown Manager register space.

Table 2: **Register Address Space**

Address (hex)	Register Name	Description
00h	CONTROL	Control register
00h	STATUS	Status register

CONTROL (Control Register – Offset 00h)

The CONTROL register is write only, and is mapped to the same address as the STATUS register.

Table 3: **Control Register**

Bit	Name	Description
31:1	Reserved	Reserved
0	request_shutdown	1 : Enter Shutdown mode 0 : Enter Pass Through mode

STATUS (Status Register – Offset 00h)

The STATUS register is read only and is mapped to the same address as the CONTROL register.

Table 4: **Status Register**

Bit	Name	Description
31:4	Reserved	Reserved

Table 4: **Status Register** *(cont'd)*

Bit	Name	Description
3	rd_in_shutdown	1: The read channel is in the Shutdown Mode 0 : The read channel is in the Pass Through mode
2	wr_in_shutdown	1 : The write channel is in the Shutdown Mode 0 : The write channel is in the Pass Through mode
1	in_shutdown	1: Both the read and write channels are in the Shutdown Mode 0 : The read or the write channel (or both) are in the Pass Through mode
0	shutdown_requested	1 : Entry to Shutdown mode has been requested 0 : Entry to Pass Through mode has been requested

Chapter 4

Designing with the Core

Responding to Transactions in Shutdown Mode

The core offers a number of ways to handle transactions that are received in Shutdown Mode:

- Terminate the transaction with a SLVERR response
- Terminate the transaction with a DECERR response
- Terminate the transaction with an OKAY response
- Hold the transaction until the core exits Shutdown Mode and then pass it on to the downstream slave. The master will not get a response until after the core exits Shutdown Mode

The best response to use depends on the target system. Although SLVERR is the correct response to use[1], it may be treated as fatal by some operating systems, and require a reboot. DECERR can have the same impact. An OKAY response is safer, but can give the false impression that the transaction completed when in fact it failed. Backpressure can cause deadlock on shared busses, cause timeouts, and can lead to transactions for one Reconfigurable Module being sent to the Reconfigurable Module that replaced it, with unknown effect.

In all cases, the core generates an interrupt to let the system know that a transaction was terminated by the core.

1. The AXI4 MM Specification states that a SLVERR should be used when “access [is] attempted to a disabled or powered-down function”.

Connecting to the Reconfigurable Partition

If the channel's AXI Master is in the Reconfigurable Module (see RP_IS_MASTER in User Parameters), then the slave side of the core (the side attached to the channel's AXI Master) is internally held in reset when in Shutdown Mode. This is to prevent spurious signals from the RM being recognised as transactions and corrupting the core. One visible effect of this configuration is that the READY signals on the slave side of the core (the ones that attach to the master interface on the RP) will deassert in Shutdown Mode.

AXI Write Channel Timing

The AXI4 protocol allows write data to be sent before the command is sent on the address channel. The Shutdown Manager core only begins processing an AXI write transaction when the command appears on the address channel. This has the following implications:

- The transaction will be sent downstream with the address and data channels aligned. Data will not be sent on before the command has appeared on the address channel.
- The data channel only has a 16 element FIFO to buffer data. Once this is full, it will stop accepting data. The upstream master must send a command on the address channel to unblock this FIFO.
- The treatment of a transaction with respect to `request_shutdown` is solely based on when the command is received on the address channel. For example, if data is received when `request_shutdown` is 0 and the command is received when `request_shutdown` is 1, the transaction will be stored with `request_shutdown` = 1, and handled by the Shutdown Manager accordingly.

General Design Guidelines

Make Only Allowed Modifications

You should not modify the core. Any modifications can have adverse effects on system timing and protocol compliance. Supported user configurations of the core can only be made by selecting the options in the customization IP window when the core is generated.

Chapter 5

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

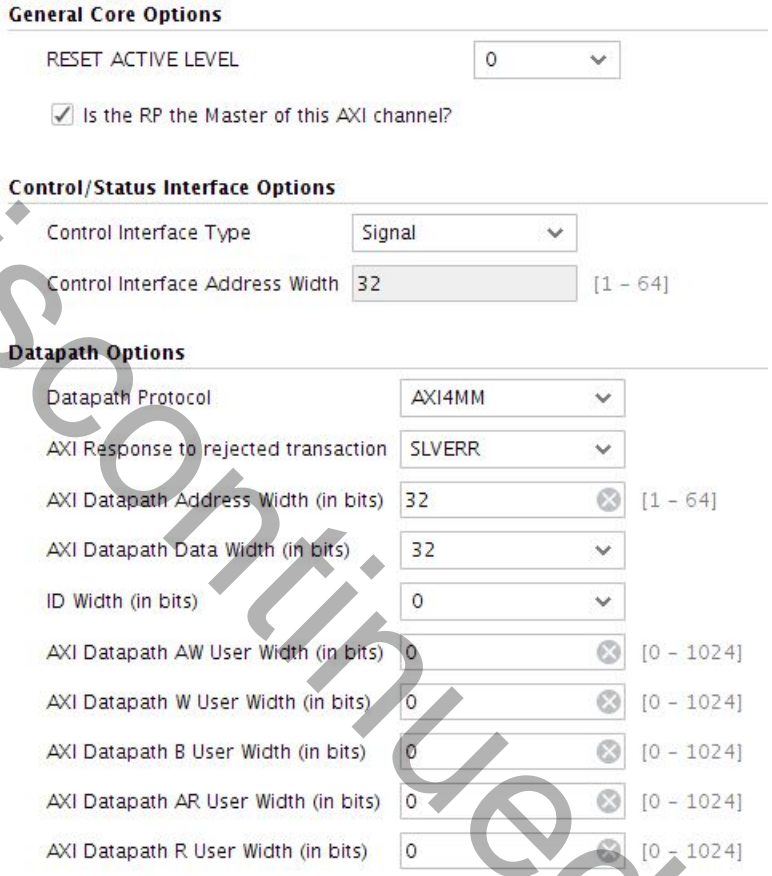
For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Customization GUI

The parameters in the customization GUI are shown in the following figure.

Figure 2: **Customization GUI**



Reset Active Level

This option sets the active level of the core reset.

0: The reset is active low, and the “resetn” signal is enabled

1: The reset is active high, and the “reset” signal is enabled

Is the RP the Master of this AXI channel?

This option specifies if the upstream AXI master is in the Reconfigurable Partition. If it is, the slave side of the Shutdown Manager is held in reset during Shutdown Mode

TRUE: The AXI Master is in the RP

FALSE: The AXI Master is not in the RP

Control Interface Type

This option enables or disables the AXI4-Lite register interface. Valid values are:

0: Disable the AXI4-Lite interface

1: Enable the AXI4-Lite interface

Control Address Width

This option sets the address width used by the AXI4-Lite register interface. Valid values are 1 to 64 inclusive.

Datapath Protocol

This option sets the protocol of the datapath. Valid values are:

- AXI4MM
- AXI4-LITE

AXI Response to rejected transaction

This option configures how the core will respond to a transaction that is received when `request_shutdown` is 1. That is, a transaction that will be handled by the core and not passed on to the downstream slave. Valid options are:

- SLVERR: Return an AXI SLVERR response
- DECERR: Return an AXI DECERR response
- OKAY: Return an AXI OKAY response

- BACKPRESSURE: Holds the transaction until the core exits Shutdown Mode. This prevents a response from being sent back to the initiating master, and causes back-pressure on the AXI bus

AXI Datapath Address Width (in bits)

This option sets the address width used by the data path. Valid values are 1 to 64 inclusive.

AXI Datapath Data Width (in bits)

This option sets the data width used by the data path. When the Datapath Protocol is AXI4MM, valid values are:

- 32
- 64
- 128
- 256
- 512
- 1024

When the Datapath Protocol is AXI4-Lite, valid values are:

- 32
- 64

ID Width (in bits)

This option sets the ID width used by the data path. Valid values are 0 to 32 inclusive. This option is disabled when the Datapath Protocol is AXI4-Lite.

AXI Datapath AW User Width (in bits)

This option sets the width of the AWUSER signal in the data path. Valid values are 0 to 1024 inclusive. This option is disabled when the Datapath Protocol is AXI4-Lite.

AXI Datapath W User Width (in bits)

This option sets the width of the WUSER signal in the data path. Valid values are 0 to 1024 inclusive. This option is disabled when the Datapath Protocol is AXI4-Lite.

AXI Datapath B User Width (in bits)

This option sets the width of the BUSER signal in the data path. Valid values are 0 to 1024 inclusive. This option is disabled when the Datapath Protocol is AXI4-Lite.

AXI Datapath AR User Width (in bits)

This option sets the width of the ARUSER signal in the data path. Valid values are 0 to 1024 inclusive. This option is disabled when the Datapath Protocol is AXI4-Lite.

AXI Datapath R User Width (in bits)

This option sets the width of the RUSER signal in the data path. Valid values are 0 to 1024 inclusive. This option is disabled when the Datapath Protocol is AXI4-Lite.

User Parameters

The following table shows the relationship between the fields in the Vivado IDE and the user parameters (which can be viewed in the Tcl Console).

Table 5: **User Parameters**

Vivado IDE Parameter/Value[1]	User Parameter/Value	Default Value
Reset Active Level	RESET_ACTIVE_LEVEL	0
Is the RP the Master of this AXI channel?	RP_IS_MASTER	TRUE
Control Interface Type	CTRL_INTERFACE_TYPE	0
Control Address Width	CTRL_ADDR_WIDTH	32
Datapath Protocol	DP_PROTOCOL AXI4MM AXI4-LITE	AXI4MM
AXI Response to rejected transaction	DP_AXI_RESP SLVERR : 0 DECERR : 1 OKAY : 2 BACKPRESSURE : 3	0
AXI Datapath Address Width (in bits)	DP_AXI_ADDR_WIDTH	32
AXI Datapath Data Width (in bits)	DP_AXI_DATA_WIDTH	32
ID Width (in bits)	DP_AXI_ID_WIDTH	0
AXI Datapath AW User Width (in bits)	DP_AXI_AWUSER_WIDTH	0
AXI Datapath W User Width (in bits)	DP_AXI_WUSER_WIDTH	0
AXI Datapath B User Width (in bits)	DP_AXI_BUSER_WIDTH	0
AXI Datapath AR User Width (in bits)	DP_AXI_ARUSER_WIDTH	0
AXI Datapath R User Width (in bits)	DP_AXI_RUSER_WIDTH	0

Notes:

1. Parameter values are listed in the table where the Vivado IDE parameter value differs from the user parameter value. Such values are shown in this table as indented below the associated parameter.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Core

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Upgrading

This appendix is not applicable for the first release of the core.

Appendix B

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the Core

AR 70697.

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address PR AXI Shutdown Manager design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
2. *Vivado Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado Design Suite User Guide: Getting Started* (UG910)
4. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
5. *Partial Reconfiguration Controller* (PG193)
6. *Vivado Design Suite AXI Reference Guide* (UG1037)
7. *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909)

Training Resources

1. Vivado Design Suite Hands-on Introductory Workshop
2. Vivado Design Suite Tool Flow
3. Xilinx Partial Reconfiguration Tools & Techniques

Revision Table

The following table shows the revision history for this document.

Date	Version	Revision
04/04/2018	1.0	Initial Xilinx release.

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