			Spartan®-6 LX FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V)							**Spartan-6 LXT FPGAs** Optimized for Lowest-Cost Logic, DSP, and Memory with High-Speed Serial Connectivity (1.2V)		
	Part Number		XA6SLX4[10,11]	XA6SLX9	XA6SLX16	XA6SLX25[10]	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T[10]	XA6SLX45T	XA6SLX75T
Logic Resources	Slices[1]		600	1,430	2,278	3,758	6,822	11,662	15,822	3,758	6,822	11,662
	Logic Cells[2]		3,840	9,152	14,579	24,051	43,661	74,637	101,261	24,051	43,661	74,637
	CLB Flip-Flops		4,800	11,440	18,224	30,064	54,576	93,296	126,576	30,064	54,576	93,296
Memory Resources	Maximum Distributed RAM (Kb)		75	90	136	229	401	692	976	229	401	692
	Block RAM (18 Kb each)		12	32	32	52	116	172	268	52	116	172
	Total Block RAM (Kb)[3]		216	576	576	936	2,088	3,096	4,824	936	2,088	3,096
Clock Resources	Clock Management Tiles (CMT)[4]		2	2	2	2	4	6	6	2	4	6
I/O Resources	Maximum Single-Ended Pins		132	200	232	266	316	280	326	250	296	268
	Maximum Differential Pairs		66	100	116	133	158	140	163	125	148	134
Embedded Hard IP Resources	DSP48A1 Slices[5]		8	16	32	38	58	132	180	38	58	132
	Endpoint Block for PCI Express®		—	—	—	—	—	—	-	1	1	1
	Memory Controller Blocks		0	2	2	2	2	2	2	2	2	2
	GTP Low-Power Transceivers		—	—	—	—	—	—	-	2	4	4
	Speed Grade		-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2	-2, -3	-2, -3	-2, -3
Miscellaneous	Temperature Grade[6]		I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
	XA Released		Q3 2011	Q3 2011	Q3 2011	Q3 2011	Yes	Yes	Q3 2011	Q3 2011	Q3 2011	Yes
Configuration	Configuration Memory (Mb)		2.7	2.7	3.7	6.4	11.9	19.6	26.5	6.4	11.9	19.6
	Package	Area										
	Chip Scale Packages (CSG): Pb-free wire-bond, chip-scale, BGA (0.8 mm ball spacing)											
	CSG225[8]	13 x 13 mm	132	160	160							
	CSG324	15 x 15 mm		200	232	226	218			190 (2)	190 (4)	
	BGA Packages (FTG): Pb-free wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)											
	FTG256	17 x 17 mm		186	186	186						
	BGA Packages (FGG): Pb-free wire-bond, fine-pitch, BGA (1.0 mm ball spacing)											
	FGG484[9]	23 x 23 mm				266	316	280	326	250 (2)	296 (4)	268 (4)

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Notes: 1. Each slice contains four LUTs and eight flip-flops.

2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT structure.

3. Block RAM are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.

4. Each CMT contains two DCMs and one PLL.

5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.

6. Temperature Range Automotive I (T_J = –40°C to +100°C); Automotive Q (T_J = –40°C to + 125°C).

7. The LX device pinouts are not compatible with the LXT devices.

8. CSG225 has memory controller support in the LX9 and LX16 devices. There is no memory controller in the XA6SLX4 devices.

9. Devices in the FGG484 have support for two memory controllers.

10. BPI configuration mode not available.

11. SelectMAP configuration modes not available.

Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

		Spartan®-3 FPGAs					Spartan-3E FPGAs				
	Part Number	XA3S50	XA3S200	XA3S400	XA3S1000	XA3S1500	XA3S100E	XA3S250E	XA3S500E	XA3S1200E	XA3S1600E
Logic Resources	System Gates[1]	50K	200K	400K	1,000K	1,500K	100K	250K	500K	1,200K	1,600K
	Slices[2]	768	1,920	3,584	7,680	13,312	960	2,448	4,656	8,672	14,752
	Logic Cells	1,728	4,320	8,064	17,280	29,952	2,160	5,508	10,476	19,512	33,192
	CLB Flip-Flops	1,536	3,840	7,168	15,360	26,624	1,920	4,896	9,312	17,344	29,504
Memory Resources	Maximum Distributed RAM (Kb)	12	30	56	120	208	15	38	73	136	231
	Block RAM Blocks	4	12	16	24	32	4	12	20	28	36
	Total Block RAM (Kb)	72	216	288	432	576	72	216	360	504	648
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	4	4	2	4	4	8	8
I/O Resources	Maximum Single-Ended I/Os	124	173	264	333	487	108	172	190	304	376
	Maximum Differential I/O Pairs	56	76	116	149	221	40	68	77	124	156
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25, LVDS33, LVPECL25, LVPECL33, Mini-LVDS25, Mini-LVDS33, RSDS25, RSDS33, TMDS25, TMDS33, PPDS25, and PPDS33					LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, and RSDS25				
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	—	—	—	—	—	—
	Dedicated Multipliers	4	12	16	24	32	4	12	20	28	36
	Device DNA Security	—	—	—	—	—	—	—	—	—	—
Miscellaneous	Temperature Grades[4]	I, Q	I, Q	I, Q	I, Q	I	I, Q	I, Q	I, Q	I, Q	I, Q
	Speed Grade	-4	-4	-4	-4	-4	Yes	-4	-4	-4	-4
	RoHS (Pb-free)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory (Mb)	0.4	1	1.7	3.2	5.2	0.6	1.4	2.3	3.8	6
Package	Footprint Area	Maximum User I/Os									
VQFP Packages (VQ): Very thin, QFP (0.5 mm lead spacing)											
VQG100	16 x 16 mm	63	63				66	66			
Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)											
CPG132	8 x 8 mm						83	92	92		
TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)											
TQG144	22 x 22 mm		97				108	108			
PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)											
PQG208	30.6 x 30.6 mm	124	141	141				158	158		
FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)											
FTG256	17 x 17 mm		173	173	173			172	190	190	
FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)											
FGG400	19 x 19 mm									304	304
FGG456	21 x 21 mm			264	333	333					
FGG484	23 x 23 mm										376
FGG676	27 x 27 mm					487					

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Notes: 1. System gates include 20%–30% of CLBs used as RAMs.

2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.

3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).

4. Temperature Range Automotive I (T_j = -40°C to +100°C); Automotive Q (T_j = -40°C to +125°C).

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			Spartan®-3A FPGAs				Spartan-3A DSP FPGAs	
	Part Number		XA3S200A	XA3S400A	XA3S700A	XA3S1400A	XA3SD1800A	XA3SD3400A
Logic Resources	System Gates[1]		200K	400K	700K	1,400K	1,800K	3,400K
	Slices[2]		1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells		4,032	8,064	12,248	25,344	37,440	53,712
	CLB Flip-Flops		3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kb)		28	56	92	176	260	373
	Block RAM Blocks		16	20	20	32	84	126
	Total Block RAM (Kb)		288	360	360	576	1,512	2,268
Clock Resources	Digital Clock Managers (DCMs)		4	4	8	8	8	8
I/O Resources	Maximum Single-Ended I/Os		195	311	372	375	519	469
	Maximum Differential I/O Pairs		90	142	165	165	227	213
	I/O Standards Supported		LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25, LVDS33, LVPECL25, LVPECL33, Mini-LVDS25, Mini-LVDS33, RSDS25, RSDS33, TMDS25, TMDS33, PPDS25, and PPDS33					
Embedded Hard IP Resources	DSP48A Slices		—	—	—	—	84	126
	Dedicated Multipliers		16	20	20	32	84[3]	126[3]
	Device DNA Security		Yes	Yes	Yes	Yes	Yes	Yes
Miscellaneous	Temperature Grades [4]		I, Q	I, Q	I, Q	I, Q	I, Q	I
	Speed Grade		-4	-4	-4	-4	-4	Yes
	RoHS (Pb-free)		Yes	Yes	Yes	Yes	Yes	Yes
	XA Released		Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory (Mb)		1.2	1.9	2.7	4.8	8.2	11.7
	Package	Footprint Area	Maximum User I/Os					
	FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)							
	FTG256	17 x 17 mm	195	195				
	Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)							
	CSG484	19 x 19 mm					309	309
	FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)							
	FGG400	21 x 21 mm		311	311			
	FGG484	23 x 23 mm			372	375		
	FGG676	27 x 27 mm					519	469

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Notes: 1. System gates include 20%–30% of CLBs used as RAMs.

2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.

3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).

4. Temperature Range Automotive I (T_J = –40°C to +100°C); Automotive Q (T_J = –40°C to +125°C).

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

			XA9500XL Family			CoolRunner™-II Family				
	Part Number		XA9536XL	XA9572XL	XA95144XL	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
Logic Resources	System Gates		800	1,600	3,200	750	1,500	3,000	6,000	9,000
	Macrocells		36	72	144	32	64	128	256	384
	Product Terms Per Macrocell		90	90	90	56	56	56	56	56
Clock Resources	Global Clocks		3	3	3	3	3	3	3	3
	Product Term Clocks Per Function Block		18	18	18	16	16	16	16	16
I/O Resources	Maximum I/O		34	72	117	33	64	100	118	118
	Input Voltage Compatible (V)		2.5/3.3/5	2.5/3.3/5	2.5/3.3/5	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
	Output Voltage Compatible (V)		2.5/3.3	2.5/3.3	2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
Speed Grades	Minimum Pin-to-Pin Logic Delay		15.5	15.5	15.5	5.5	6.7	7	7	9.2
	Automotive I Speed Grades		-15	-15	-15	-6	-7	-7	-7	-10
	Automotive Q Speed Grades		-15	-15	-15	-7	-8	-8	-8	-11
Miscellaneous	Temperature Grades[1]		I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
	RoHS (Pb-free)		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Package	Area[2]	Maximum User I/Os							
	VQFP Packages (VQ): Very thin QFP (VQG44: 0.8 mm lead spacing; VQG64 and VQG100: 0.5 mm lead spacing)									
	VQG44	12 x 12 mm	34	34		33	33			
	VQG64	12 x 12 mm		52						
	VQG100	16 x 16 mm					64	80	80	
	TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)									
	TQG100	16 x 16 mm		72						
	TQG144	22 x 22 mm							118	118
	Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)									
	CPG132	8 x 8 mm						100		
	Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)									
	CSG144	12 x 12 mm			117					

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Notes: 1. Temperature Grade XA CPLD Automotive I (T_A = –40°C to +85°C); Automotive Q (T_A = –40°C to +105°C with $T_{J\ MAXIMUM}$ = +125°C).
2. Area dimensions for lead-frame products are inclusive of the leads.