XILINX

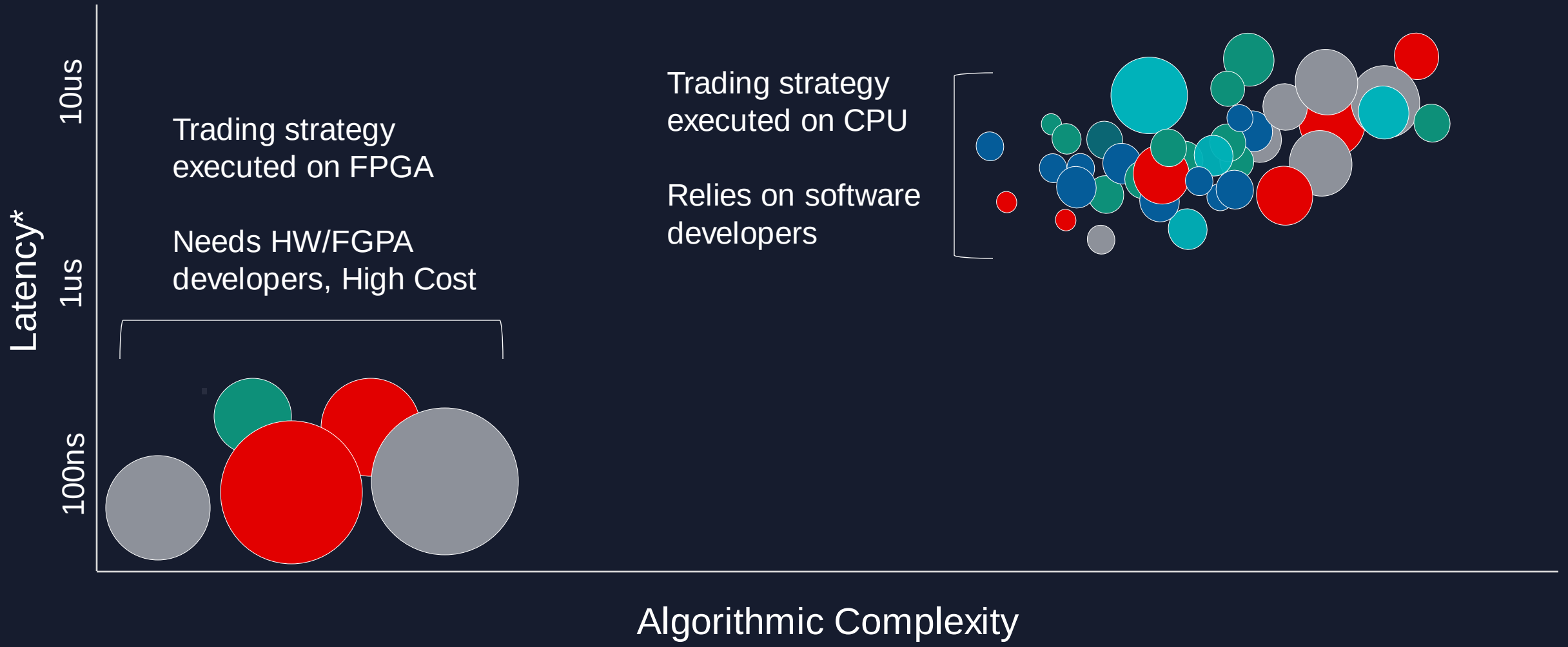
Xilinx Accelerated Algorithmic Trading

Hardware Accelerated Algorithmic Trading Made Easy

Hamid Salehi

March 2021

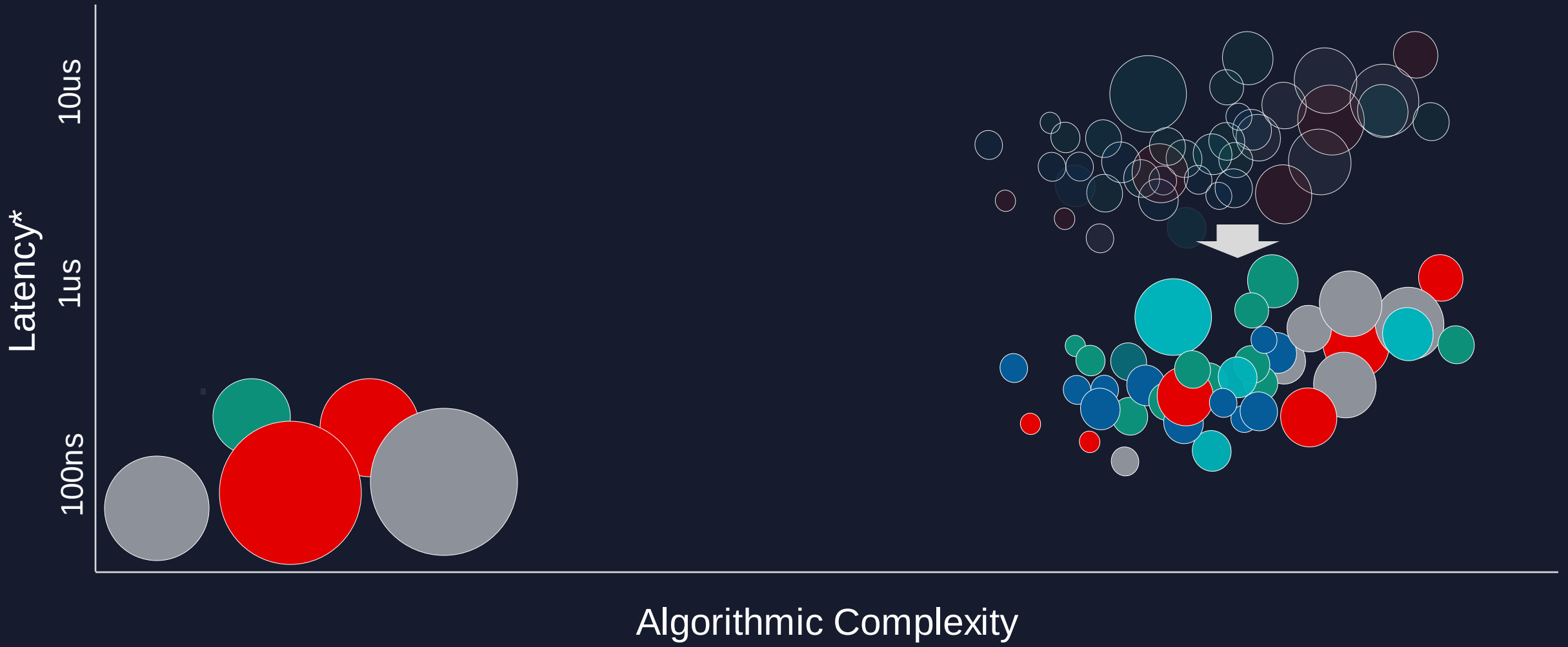
Algorithmic Trading Today



* Latency for trading is defined as the time duration from the moment a security price appears and the moment a trade is executed

XILINX.

The Challenge: Reduce Latency Without HW Design



XILINX.

Introducing Xilinx Accelerated Algorithmic Trading (AAT)

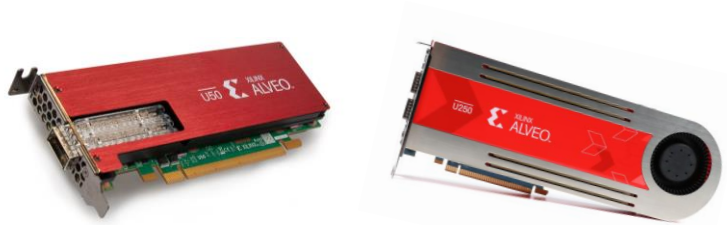
Customizable, open-source trading reference design with sub-microsecond latency

XILINX VITIS™

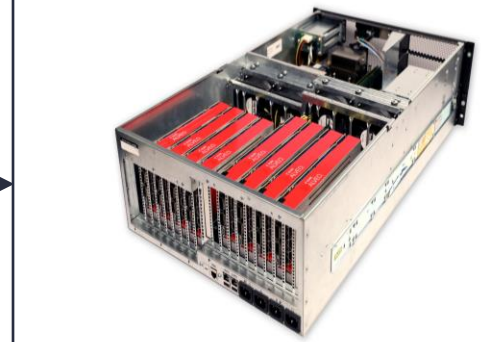
Software Platform

Fully customizable using standard libraries and C/C++

ATT Reference Design

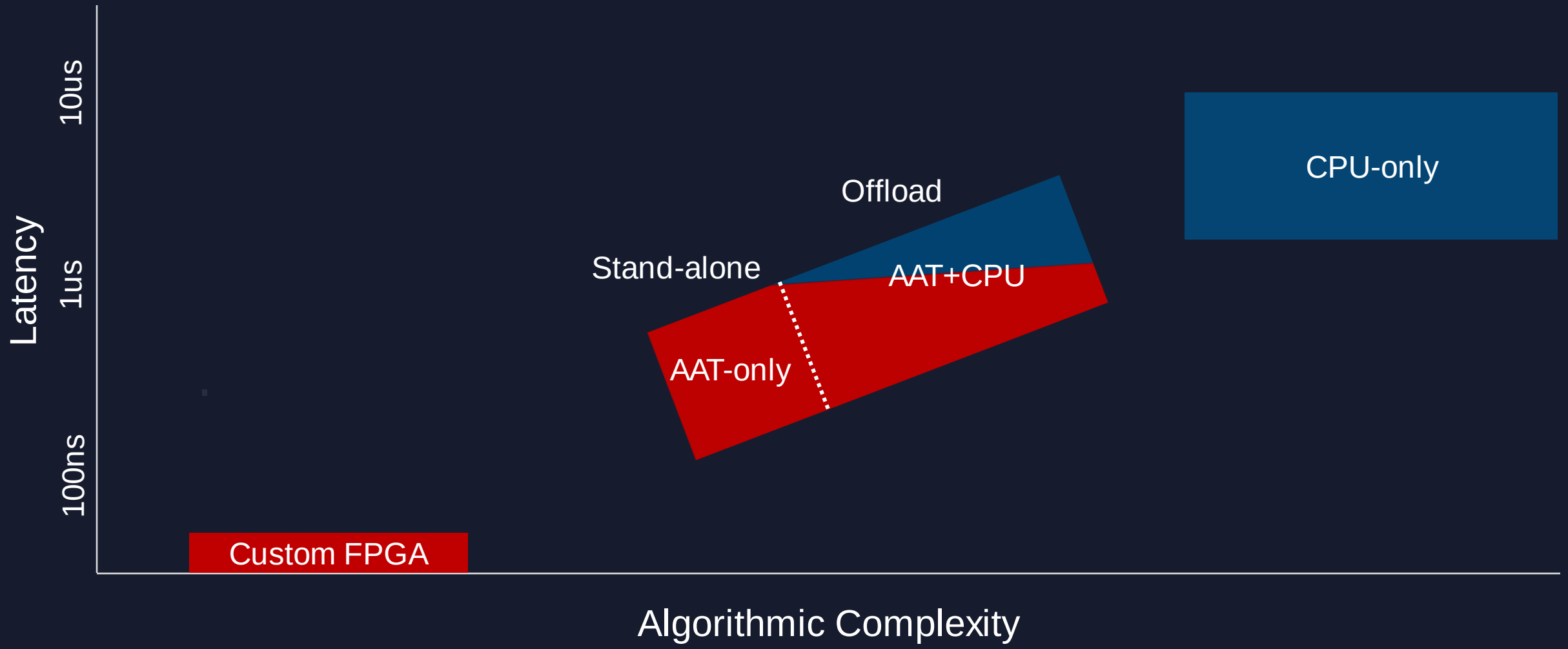


Can be implemented on Xilinx Alveo U250, U50 cards



XILINX

Use AAT as Standalone Accelerator or for CPU Offload



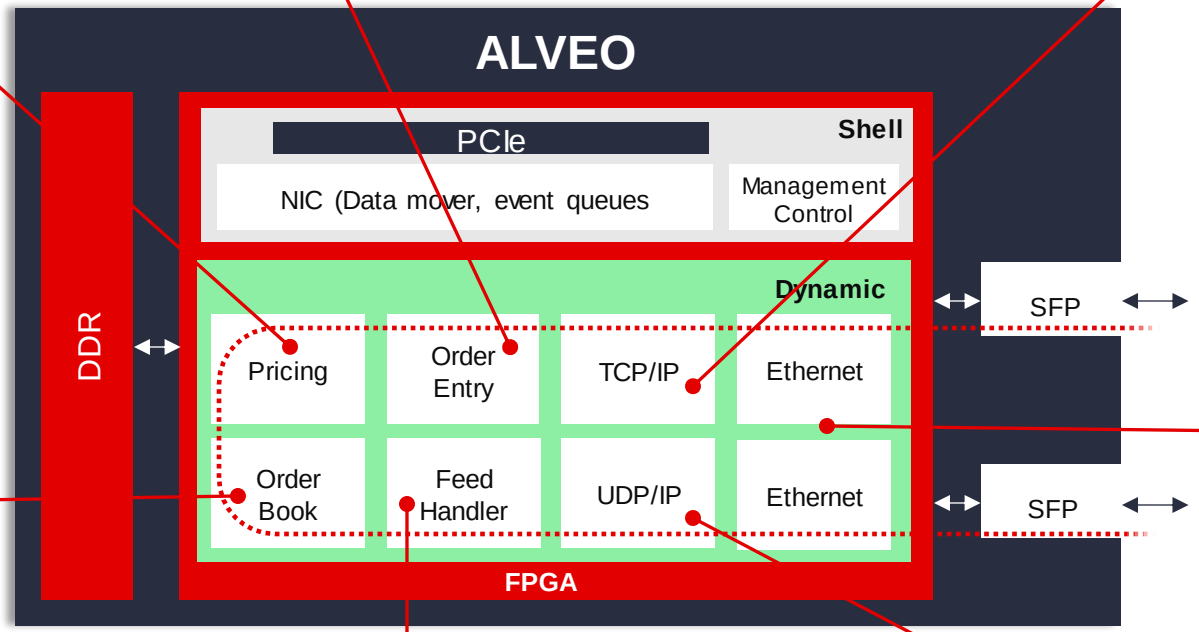
XILINX.

ATT Modular Design Explained

Pricing: Triggered by changes in the orderbook, generates requests for orders to the exchange

Order Entry: Creates market request orders in the appropriate format to send to the exchange.

TCP/IP : Establishes and maintains a TCP session to the exchange & manages transfer of orders placed



Orderbook: Implements a five-level orderbook based on a CME market by price system (Bid & Ask).

MAC: The 10G/25G Ethernet Subsystem IP performs MAC termination and 66b PCS layer processing for TCP and UDP frames.

FeedHandler: Parses frames & filters packets based on the ticker symbol.

UDP/IP: Terminates incoming UDP packets from the exchange and recovers the payload

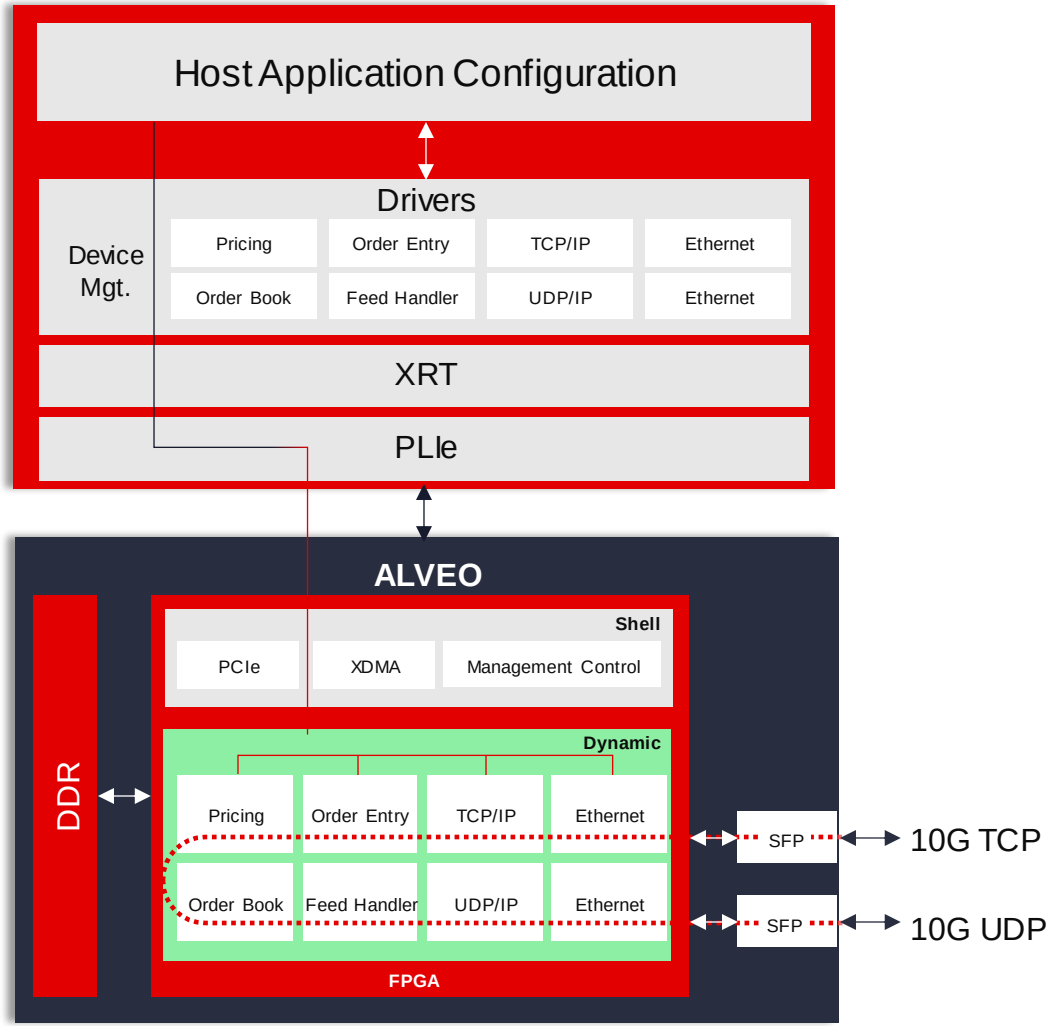
Each module can be used as is, or customized to create a tailored trading solution

XILINX.

Designed to accelerate migration from CPU to FPGA

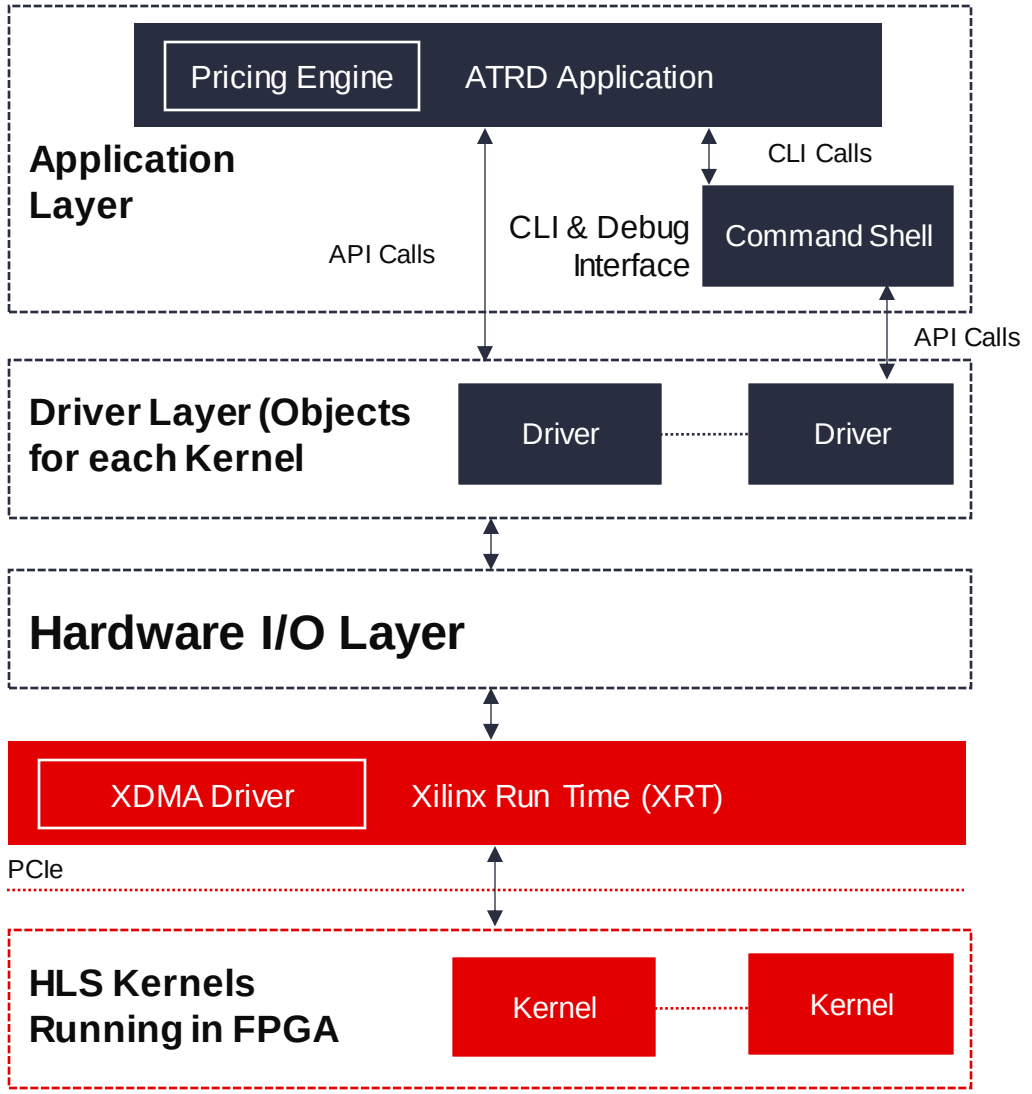
The building blocks to enable software development of an electronic trading system on Xilinx Alveo products

- ✓ Fully written in HLS
- ✓ Designed for Software Engineers
- ✓ Integrated with Vitis
- ✓ Runs out the box on Xilinx Alveo
- ✓ Example HLS Code provided



Software Overview of AAT Reference Design

- Application Layer
  - Command shell provides easy interface with help functionality
- Driver layer (User space)
  - One driver for each kernel running on FPGA
- Hardware I/O Layer
- XRT (Xilinx Run Time)
- HLS kernels running on FPGA



Who Can Benefit From AAT Reference Design

BROKERS

EXCHANGES

MARKET DATA VENDORS

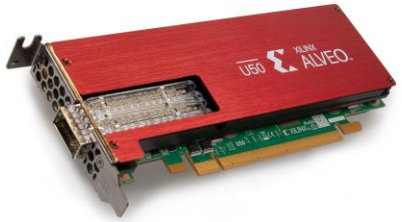
SELL SIDE VENDORS

PROPRIETARY TRADERS

Pre-Trade Risk | Tick To Trade | Algorithmic Trading | Smart Order Routing | Market Data Accelerator | FIX Gateway

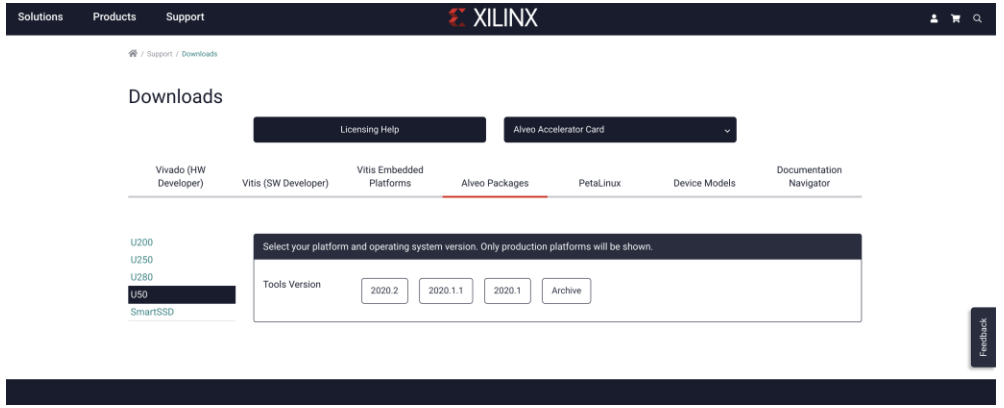
Get Started With Xilinx Accelerated Algorithmic Trading

Regain the latency edge



Alveo U50 & U250 - available through Xilinx VARs and VADs

+



Free open-source download from Xilinx.com, no license fees

www.xilinx.com/applications/data-center/financial-technology/accelerated-algorithmic-trading.html

XILINX

Thank You