

4K TV Development Made Easy with the Zynq SoC

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4K

Xilinx All Programmable technology can be a boon for designers of 4K video systems. Associated tools, IP and reference designs will help those new to FPGA design.

Ultrahigh-definition (UHD) TVs, also called 4K for their resolution level, are already widely available and 4K is proving a much more popular technology than 3D TV among consumers. But

the standards lag behind the uptake. Society of Motion Picture & Television Engineers (SMPTE) standards for 6-Gbps and 12-Gbps SDI, supporting 4K60 video, are only just being released, while HDMI™ 2.0 and DisplayPort supporting the same resolution are in the early stages of adoption. Given the significant consumer demand for 4K UHD TVs, many ad hoc standards have rushed in to fill the void.

Indeed, so much about 4K UHD TV is in a state of flux that it is essential for systems to be flexible enough to adapt to the developing standards. The way to ensure flexibility is to replace the time-honored chip sets and ASSPs long used for these designs with FPGAs and All Programmable systems-on-chip such as the Xilinx® Zynq®-7000 All Programmable SoC. These solutions offer the flexibility needed while also delivering performance comparable to that of ASICs.

At the same time, the size and performance of the latest FPGAs and SoCs present considerable design challenges, especially to engineers who are not particularly FPGA-savvy. While there are many similarities in the design of hardware and FPGA implementations, FPGA-based systems typically involve many more components. In addition, the inherent flexibility of firmware designs introduces extra complications.

Fortunately, Xilinx offers a lot of help for 4K TV designers—all at a much lower cost in both time and money than designing your system from scratch. But before delving into the details of how to use FPGA technology for 4K applications, let's first take a look at how 4K systems have managed to become so popular so quickly, and the issues that any 4K system has to address.

THE UPSIDES AND DOWNSIDES OF 4K

Ever since television was first invented, there has been a constant drive toward making the images it shows closer to real life. This effort typically comes down to providing bigger, better and faster video by increasing the resolution,

the frame rate or the dynamic range of the images (that is, how bright they can be)—plus, of course, attempting to achieve either a true 3D effect or at least a more immersive feel.

Increasing the resolution allows the images to be more detailed and makes it possible to display them on larger screens without the pixelation becoming obvious. Bigger screens give a more immersive feel. These are improvements that customers find easy to appreciate and hence, are willing to spend money on. The improvements brought about by increasing the frame rate (smoother motion) or the dynamic range (brighter lights and darker blacks), while compelling, have been slower to capture the consumer's imagination so far.

The new 4K UHD TV represents a quadrupling of the number of pixels from the previously sought-after HD standards. Perhaps most important for customers, 4K allows them to upgrade to a much larger TV that offers a much more immersive feel without any obvious effect on the image quality.

There are, however, plenty of technical challenges intrinsic to developing systems to support 4K video. For a start, a frame size of 3,840 x 2,160 pixels delivered at frame rates of up to 60 Hz represents a 600-MHz pixel rate. It takes a very high-performance system to process this rate in real time. Then there are the different delivery configurations that are being

defined for 4K—all involving multiple data streams, some delivered multiplexed on the same cable, some on different cables—and the different technologies emerging to supply them: 4x3G; 6G-SDI and 12G-SDI; HDMI 1.4 and 2.0; DisplayPort 1.2; and V-by-One HS.

Another issue for designers is the need for any system to handle not just 4K but also many if not all of the video standards currently in use, including SD. In addition, the system must support conversion among these different standards with all the associated issues of up/down/cross-conversion, nonmatching color spaces, color correction, interlacing and deinterlacing, and cadence handling. An additional complication is that upconversion typically also needs to be followed by the application of so-called “super-resolution” enhancement techniques to counteract the image smoothing that inevitably results.

Other processes that may be needed include noise reduction, cropping and resizing—all to be done in real time. Some systems may also need to handle High-Bandwidth Digital Copy Protection (HDCP).

Furthermore, anyone needing to determine the quality of the broadcast transmissions will also need to generate appropriate eye and jitter displays, the technology for which becomes increasingly difficult to implement at higher bit rates.

FIRST LEVEL OF ASSISTANCE: 4K IP CORES

The first step in designing any system is to find ready-made blocks that you can usefully include in your design. In the FPGA world, the equivalent building blocks to the various chips available for inclusion in a PCB design are intellectual-property (IP) cores. So your first step is to identify what IP cores are available for use in your 4K UHD design.

OmniTek is a good source of IP cores for all types of video system design. The company, which is a certified member of the Xilinx Alliance Program, has a depth of experience in video processing, initially as developer of its own video test-and-measurement (T&M) systems. These systems needed dedicated hardware, which in turn led to the development of dedicated firmware blocks. Those firmware blocks are now also available as IP cores. The creation of OmniTek's latest T&M system, the newly launched Ultra 4K Tool Box, led to the development of a range of 4K-capable IP cores, now available to third-party developers.

Two cores in particular are useful to designers of 4K systems: OmniTek's OSVP v2 Scalable Video Processor and its Multi-Channel Streaming DMA Controller, both of which are available targeted for Xilinx 7 series FPGAs and Zynq SoCs. Both cores adopt the ARM® AMBA® AXI4 system interconnect standards.

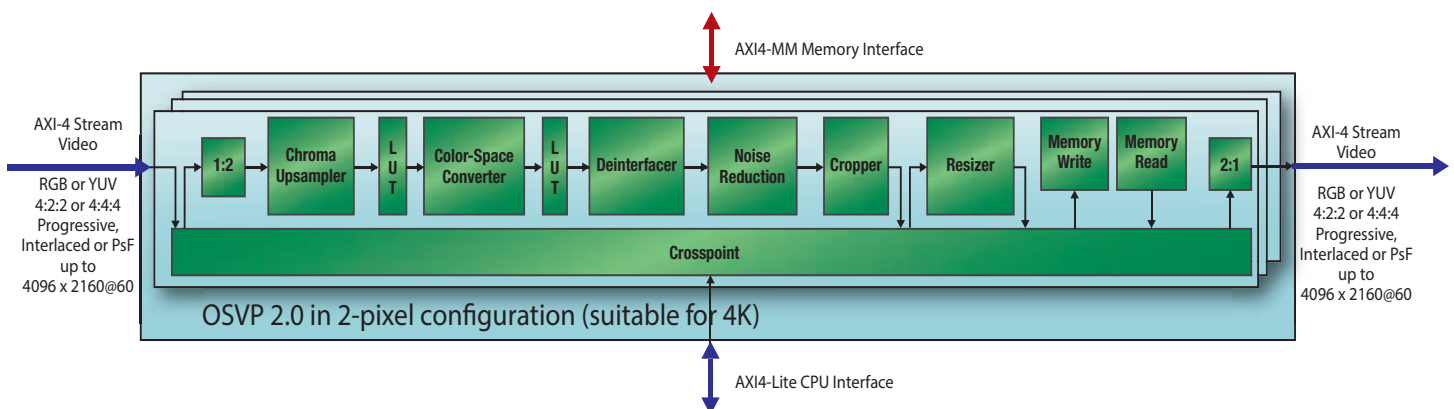


Figure 1 – Input channel architecture of OmniTek's OSVP v2 Scalable Video Processor core

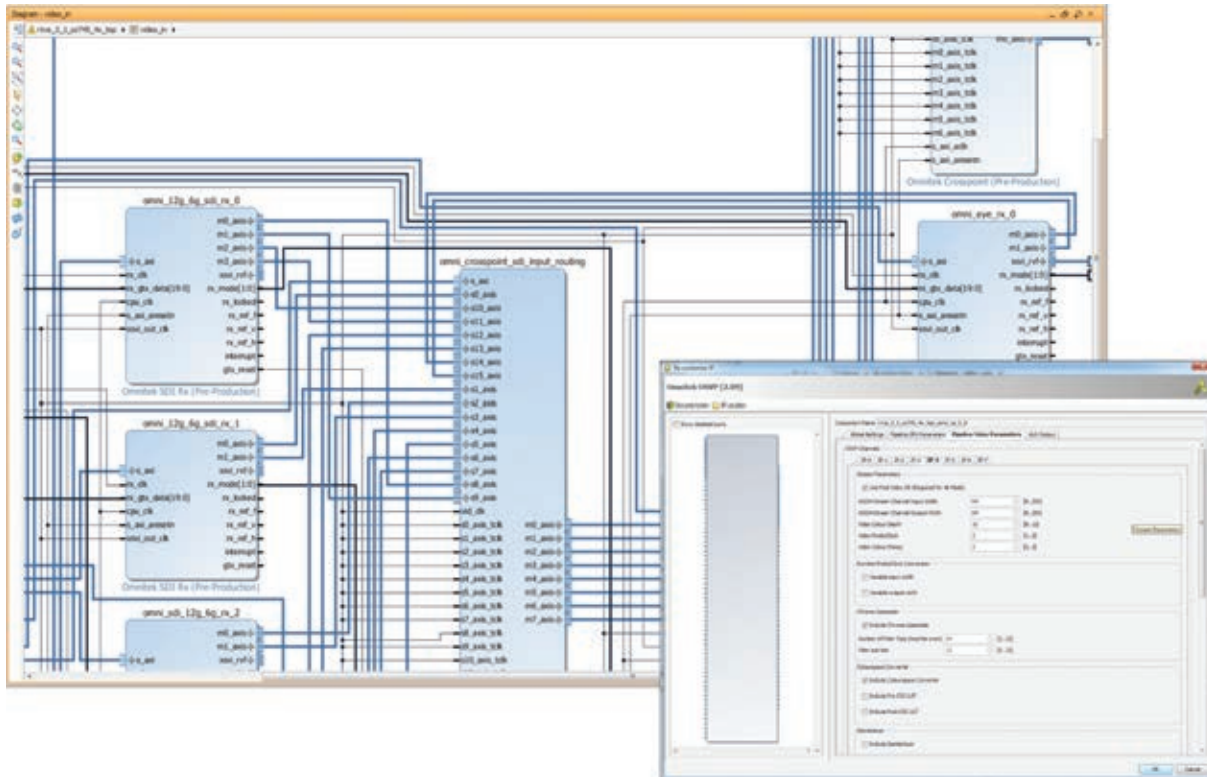


Figure 2 – The RTVE 3.1 video design as laid out within Vivado IP Integrator, together with Configuration window

The OSVP v2's facilities include six-axis color correction; motion- and edge-adaptive deinterlacing (complete with 3:2 and 2:2 film cadence detection and processing); the ability to resize and crop with image sharpening and smoothing; and noise reduction. Figure 1 shows a block diagram of this core. You configure the selection of processing facilities that are included at compile-time, while further details of the processing carried out by the OSVP v2 core can either be set at run-time or driven from software.

The OSVP v2 core comes as part of a suite that also includes a combiner for combining multiple video streams; an interlacer for producing output in interlaced formats; a dedicated crosspoint; and a chroma resampler that you can use to migrate between 4:4:4, 4:2:2 and 4:2:0 YCbCr. (A single implementation of the chroma resampler is able to convert from 4:4:4 to 4:2:2; from 4:2:2 to 4:2:0; from 4:2:2 to 4:4:4; or from 4:2:0 to 4:2:2.)

A single OSVP v2 core can process multiple video channels. The limiting factors are the resources offered by the FPGA or SoC on which it is implemented and the amount of SDRAM bandwidth available. For example, you could configure an OSVP core implemented on a Kintex®-7 XC7K325T FPGA to support up to eight inputs handling video at eight different HD video standards, eight color spaces and so on. At the same time, you could configure the output block for up to 16 progressive HD outputs. Alternatively, you could set up the output block to offer either a single 4K channel or a set of four channels that together offer Square Division ("quad") or 2-Pixel Sample Interleave 4K.

Another challenge for those designing complex 4K systems is managing the many high-bandwidth memory accesses required in processing video. Sometimes the required video handling is offered alongside the video-processing block. For example, the OSVP v2 core includes a Multi-Port Video DMA

block that provides a highly efficient engine for handling video input/output.

Capturing and playing out one or more channels of 4K60 over PCI Express®, however, requires a DMA controller optimized for handling streaming data across a PCIe® interface. OmniTek's Multi-Channel Streaming DMA Controller has a couple of key features to help here. The first is FIFO-based DMA (FDMA), which bypasses the need to transfer the data in and out of memory. The second is a series of design optimizations that allow the controller to make highly efficient use of the PCIe bandwidth, such as by prefetching of scatter-gather-mode descriptors and back-to-back packing of TLP packets.

Another IP core that OmniTek has developed for working with 4K UHD video is a block for unraveling the different streams that make up two-sample interleave forms of 4K video. Also, a drop-in replacement for the basic MIG SDRAM controller further improves the performance for UHD TV video applications.

THE PROGRAMMABLE ADVANTAGE

Further support for designers of FPGA- and SoC-based 4K video systems comes from Xilinx and it comes in three forms.

The first advantage resides in the Zynq SoC, a device that provides a powerful combination of hardware and software processing capabilities for high-performance video or image processing. The Zynq SoC integrates a feature-rich dual-core ARM Cortex™-A9 processing system with 7 series (28-nanometer) FPGA programmable logic in a single device. Users can either run processing algorithms on the ARM processors or offload them into FPGA hardware when acceleration is needed to achieve real-time operation.

The 300-MHz sustainable video-processing speed offered by the programmable logic of both Kintex-7 FPGAs and the Zynq SoC, combined with a

memory performance of 64-bit DDR3 at 1,600 Mbps, is critical for handling 4K video processing and 4K frame buffers. The Zynq SoC's DSP-rich programmable logic fabric gives DSP designers a highly flexible platform on which to implement signal-processing algorithms, while the tight coupling between the processor and the programmable logic allows the development of codec algorithms across both domains. Basing a design on a Zynq SoC also saves power and cost, since you are able to integrate in a single device what would otherwise take multiple ASSPs to accomplish.

Xilinx also offers significant connectivity support to enable 4K video system development, both through the range of built-in transceivers included on its FPGAs and SoCs and through its broad range of in-house connectivity IP. The Zynq 7045 SoC,

for example, offers up to sixteen 12.5-Gbps transceivers, allowing its use in conjunction with the 12G-SDI, 6-Gbps HDMI 2.0, 5.4-Gbps DisplayPort 1.2 and 10-Gbps Ethernet standards.

The third important contribution Xilinx makes is through the IP Integrator (IPI) tool associated with the Vivado® Design Suite. As illustrated in Figure 2, with the IPI, the task of linking IP blocks becomes similar to linking up chips on a printed-circuit board. It becomes particularly easy where (as with the OmniTek OSVP and DMA blocks) the interfaces on the IP blocks conform to the AMBA AXI4 interconnect protocols, which Xilinx has adopted as standard.

Even more power is available with the advent of Xilinx's new UltraScale™ (16-nm/20-nm) technology, which supports clock speeds up to many hundreds of gigabits per second and is being described as "ASIC-class." (For

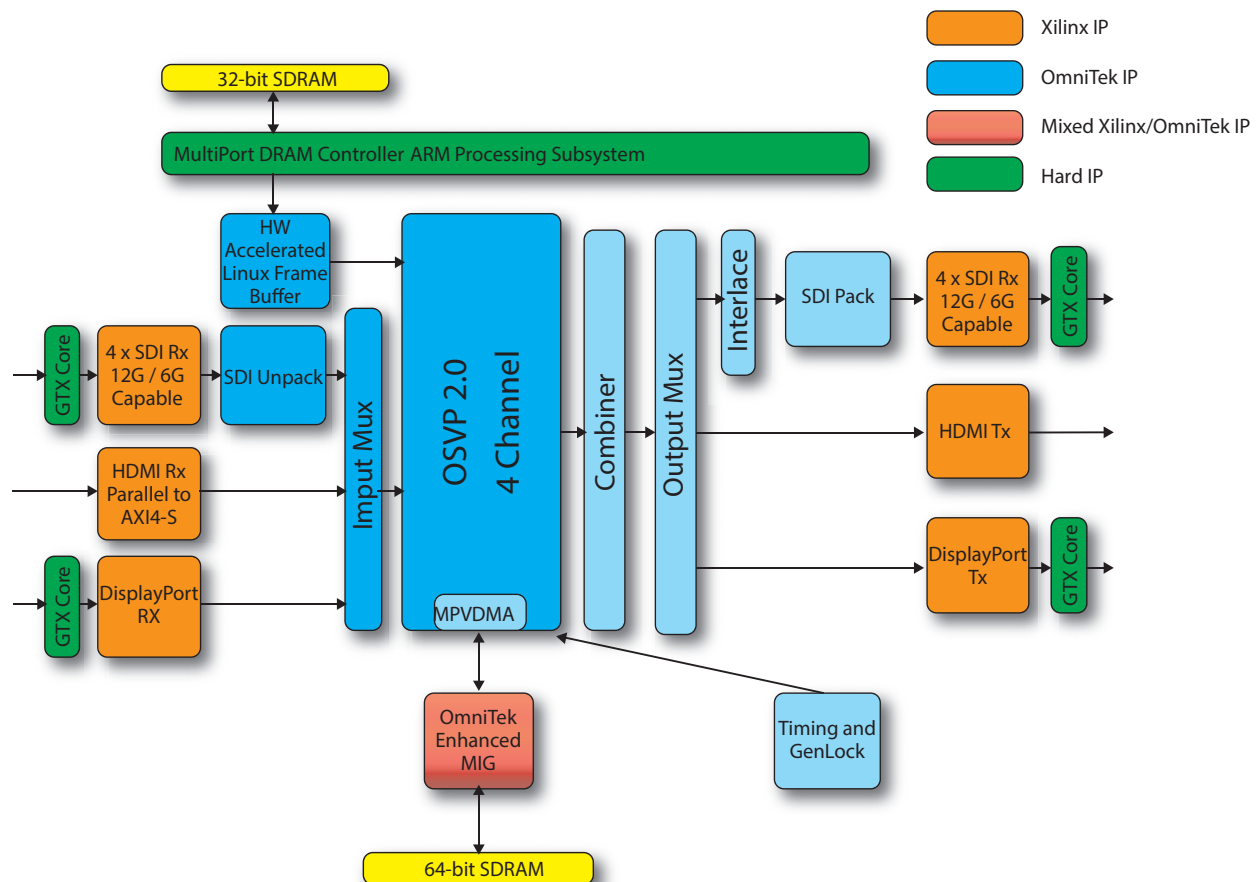


Figure 3 – Outline structure of the RTVE 3.1 Reference Design



Figure 4 – OmniTek's new Ultra 4K Tool Box, shown open to reveal the components upon which it is based

further information, see www.xilinx.com/products/technology/ultrascale.html). The UltraScale architecture enables the development of video systems not only at 4K but also beyond, with 8K on the horizon.

READY-MADE SYSTEMS TO ADAPT

While the building blocks offered by IP cores go a long way toward easing the task of creating video system designs, ready-made systems that you can adapt provide an even better starting point. For some time, Xilinx has been offering Real-Time Video Engine (RTVE) reference designs incorporating both Xilinx video and connectivity IP and IP blocks from OmniTek. These reference designs provide highly demonstrable, broadcast-quality video processing targeted to a wide range of video applications. The RTVE designs demonstrate both the functionality of these IP blocks and their easy interoperability, because they have all been designed to AXI4 interconnect standards.

Each new version of RTVE has extended the capabilities of the design by incorporating the latest IP blocks. The most recent version—RTVE 3.1—adds support for 4K video standards as defined by SMPTE 425-5:2014, DisplayPort 1.2, 6G-SDI and 12G-SDI. Figure 3 outlines the block diagram for this design.

The RTVE 3.1 design incorporates both of the OmniTek cores described above, along with the OmniTek interlacer, combiner and dedicated cross-point and some key components from Xilinx. It also comes with an API and an application to drive the RTVE engine from a Web-based interface. Both the firmware of the RTVE 3.1 design and the software of the application are available to customers in source form for use either as an illustration of how to go about designing a system using these tools or as the starting point for developing similar systems.

Also available to customers is the hardware platform for the RTVE 3.1, which comprises the OmniTek OZ745 Development Kit (based around a Xilinx

Zynq 7045 SoC) and an FMC expansion card. The FMC adds DisplayPort 1.2-compatible input and output ports, along with two SD/HD/3G/6G-SDI inputs and outputs. Together, those I/Os make it possible to extend the video standards supported to include 6G 4K and 12G 4K; 3G Level A and 3G Level B Square Division/Quad 4K; and 3G Level A and 3G Level B 2-Sample Interleave 4K.

The proof that these components can be used together to create a commercially viable system comes in the form of OmniTek's Ultra 4K Tool Box (Figure 4). The basic architecture of this 4K Tool Box is built around OmniTek's OZ745 Development Kit, FMC card and the firmware and associated application software of the RTVE 3.1. The 4K Tool Box not only provides up-, down- and cross-conversion of all video standards up to 4K60 and associated image correction, but also offers a wide range of displays including eye and jitter, gamut views and pixel data across all the many data streams that make up 4K images.

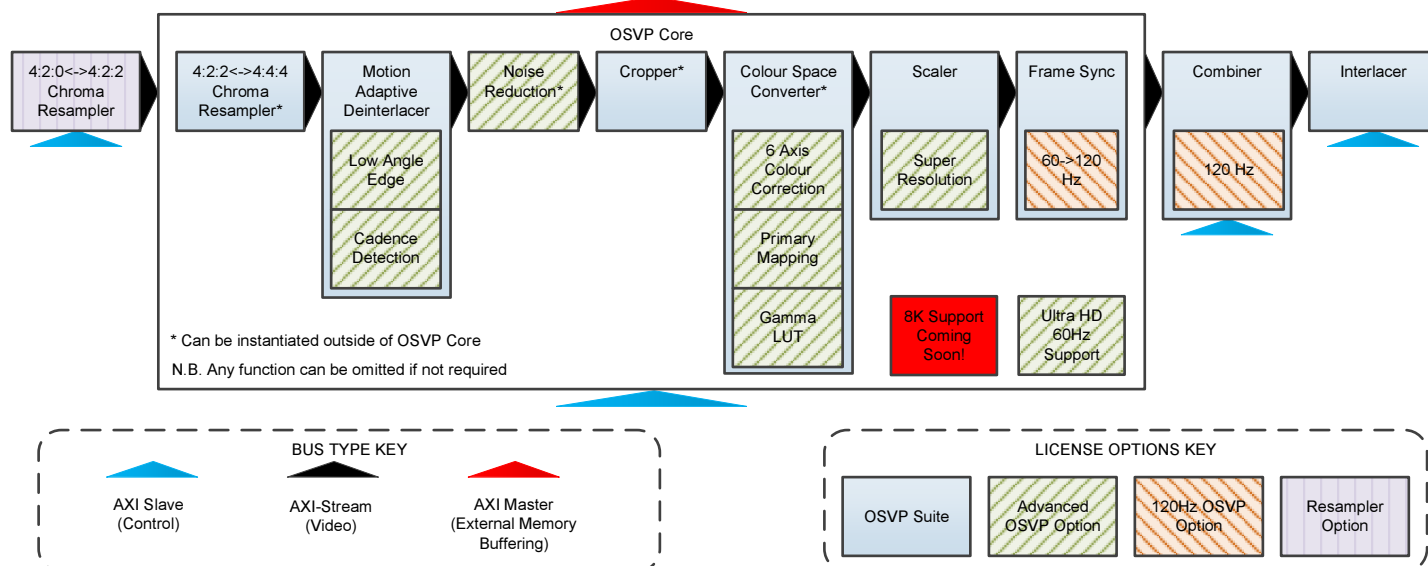
The Ultra 4K Tool Box is newly on the market but has already been purchased by a broad spectrum of customers, covering all areas of 4K processing from chip-set manufacture to test and measurement and broadcast. The uptake demonstrates the real interest in the new 4K standards across the video industry.

THE ULTIMATE ASSISTANCE

Along with these tools and IP, OmniTek also offers consultancy services to help customers get 4K designs up and running. The combination of leading-edge silicon technology and software tools from Xilinx and the video-processing and manufacturing expertise from OmniTek means that a designer of a video system starts within a complete development framework, with much easier integration capabilities and better support than they might have expected. The result is the muscle to get innovative and competitive products to market much more quickly. 🌟

OSVP Scalable Video Processing Suite Omnitek for Xilinx® FPGAs and SoCs

A highly configurable set of IP blocks and optional features that together provide a powerful range of tools for multi-video format conversion and image enhancement for video formats up to 60Hz Ultra HD, with 120Hz Ultra HD output as a further option. For ease of implementation and to make best use of system resources, the principal IP blocks are packaged as a single 'OSVP' core offering up to 8 video channels that you can individually configure to carry out the precise range of actions needed to deliver the transformations you require.



Key Features

- Support for:
 - Video input formats up to 4096 x 2160 60Hz; output formats up to 4096x2160 120Hz
 - Interlaced, progressive or segmented frame (PsF) input; progressive or interlaced output
 - YUV and RGB colour in 4:2:0, 4:2:2 or 4:4:4 format
 - 8-, 10- or 12-bit colour depths
 - Up to 8 video processing paths, each individually configured with regard to video standard and the processing actions carried out
- Full 12-bit YUV or RGB 4:4:4 processing, providing:
 - Up/Down/Cross conversion between any supported standards
 - Asynchronous input and output timing with frame synchronization
 - Frame synchronous transitions when changing frame rate
 - Chroma re-sampling
 - Full 6-axis YUV/RGB colour correction, brightness and saturation level control, and hue rotation
 - Colour primary mapping
 - Motion- and/or Edge-adaptive de-interlacing with best-in-class low-angle handling
 - 3:2 and 2:2 film cadence detection and processing, including handling of mixed cadence such as interlaced video over 3:2 film
 - Noise reduction
- Crop and resize with Super-Resolution image enhancement
 - Alpha blending of multiple video sources
- Provided ready for use in Xilinx Vivado IPI Design Environment
 - Resource use and signal timing optimised through packaging the main processing blocks as single configurable 'OSVP' core
 - AXI4-Stream interfaces for video; AXI4-MM to SDRAM controller; AXI4-Lite to control registers
 - Omnitek FPGA Software Interface Framework for easy prototyping, with drivers for Linux and Xilinx Kernel that present identical APIs.
 - All blocks optimised for Xilinx FPGA technology



Chroma Resampling

Chroma resampling may be needed both to up-sample the incoming video stream to the 4:4:4 format used for signal processing throughout the OSVP core and to deliver the required output video format.

The OSVP Suite includes 4:2:2 to 4:4:4 and 4:4:4 to 4:2:2 resamplers as standard. 4:2:2 to 4:2:0 and 4:2:0 to 4:2:2 Chroma resamplers are available as an add-on to the OSVP Suite. All four resamplers may be used alongside the OSVP core or instantiated independently as required

Deinterlacing

Interlaced and PsF format inputs need to be deinterlaced prior to signal processing. However special care is needed in order to avoid generating artefacts, particularly where the video includes motion or low-angle edges. Failure to detect film cadences correctly will also give rise to artefacts in the deinterlaced video stream.

Motion-Adaptive Deinterlacing and Low-Angle Edge Correction are provided as standard, but with the 'Advanced' option, the OSVP benefits from the use of the application of some highly-sophisticated algorithms, particularly in the areas of Low-angle Edge Detection and Film Cadence Processing. The Film Cadence Processing is able to handle 3:2 and 2:2 file cadences for all types, together with mixed cadence material such as interlaced text overlaid on a 3:2 film cadence..

Cadence Detection



Failure to detect film cadences gives rise to spurious artefacts both in 2:2 cadence material (top) and 3:2 cadence material (bottom).

Responsive film cadence detection allows the original material to be recovered without artefacts.

Enhanced Motion/Low-Angle Edge Detection



Simple line interpolation gives rise to jaggy artefacts and flickering static content.

With advanced low angle edge interpolation and motion detection, the jaggy artefacts are removed and static content is enhanced.

Video over Cadence:



Failure to detect where areas of interlaced video content are overlaid on a 3:2 film cadence gives rise to combing artefacts.

Correct detection allows these areas to be correctly deinterlaced whilst recovering the original film material.

Noise Reduction

Before an image is upsized, it is advisable to remove any noise or stuck pixels. The OSVP Suite 'Advanced' option adds Noise Reduction to the range of facilities offered by the OSVP core. Noise is reduced by applying a variable statistical filter to the signal. This approach achieves good results with both specular noise and stuck pixels.



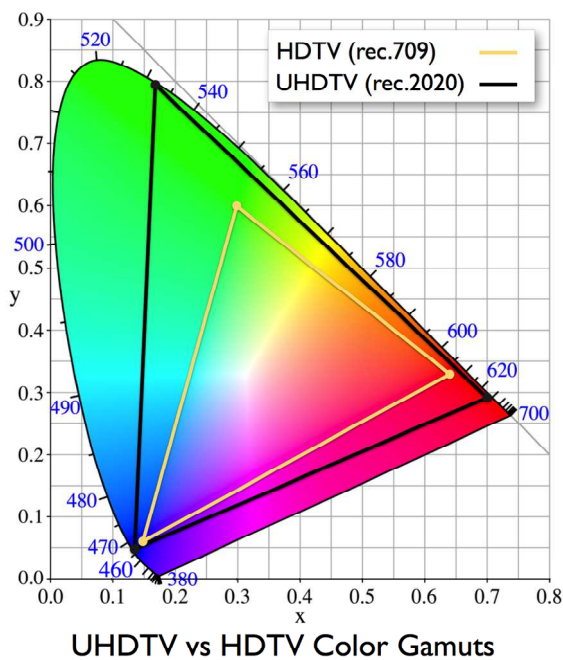
The speckling that results from noisy content can be very distracting, especially when the image is upsized.

Noise reduction filtering reduces both the speckling effect and the number of stuck pixels while maintaining important details.

Colour Space Conversion and Colour Primaries

A necessary part of transforming video is the mapping of pixel data between colour spaces in order to preserve the colouring of the content. This mapping is required because the different formats define different sets of primary colours. For example, SD uses the Rec 601 set of colour primaries, while HD follows Rec 709 and UHD follows Rec 2020. Each display device also uses a particular set of primary colours.

(The marked difference between the colour spaces used by these standards is illustrated by the diagram shown {{somewhere: currently below}}. The two triangles formed by joining the Colour Primaries for HD (Rec 709) and UHD (Rec 2020) enclose the colour spaces defined for these two formats.)



UHDTV vs HDTV Color Gamuts

The OSVP's Colour Space Conversion block enables pixel data to be transformed between any input colour space and any output colour space. All that is needed is the three primary colours and the white point associated with each colour space. The colour spaces need to be accurately defined: any errors in their definition will result in a poor colouration.

The OSVP Colour Conversion block supports standard colour spaces such as those defined for SD, HD and UHD. With the Advanced option, it also supports user-defined colour spaces, allowing detailing of the colour space used by a particular display device. It also offers gamma correction, allowing the correction of any gamma that may have been applied.



Using the wrong colour primaries gives results that are poorly coloured.



Mapping the colour primaries correctly ensures the original colouring is preserved.



In the absence of gamma correction, some areas of the image can be either excessively dark while other are excessively light.



The flexible gamma correction offered by the OSVP core allows mapping between input and output gamma curves.

6-Axis Colour Correction

A further level of colour change is brought about by applying Gain and/or Lift to the individual colour components. This is added to the OSVP by the Advanced option and provides individual Gain and Lift controls for each of the six colour RGB and YUV components. Controls are also offered for Overall Brightness, Saturation level and Hue Rotation. Out-of-range values are automatically clipped.



6 Axis Colour Correction allows you to make both RGB and YUV lift and gain adjustments.



Brightness, Saturation and Hue can be used to swap colours and enhance their presence.



They can also be used to simulate photographic effects such as sepia-toning.

Resizing Images

Moving between different resolutions and compositing several source images into a single image typically requires images to be resized. The OSVP Resizer allows images to be compressed or expanded across the full range of image resolutions. Moreover the technique used makes highly efficient use of the underlying FPGA/SoC's DSP resources.

Crop and Aspect Ration Conversion



Resizing content with different aspect ratios incorrectly can result in compression or stretching.

Flexible cropping and resizing enables aspect ratios to be maintained. Pan and scan can also be supported.

The process of resizing an image is however prone to introducing a range of unwanted effects. For instance, the result of upscaling an image often appears softened. Another common effect is 'ringing' near edges. Adding the Advanced option to the OSVP adds a range of 'Super-Resolution Enhancement' algorithms that both counteract these effects and offer different levels of smoothness or sharpening in the end result.

Super Resolution Enhancement



Upscaling to UHD resolution can introduce blurred content or ringing artefacts.



Using advanced filtering techniques allows detail to be enhanced and ringing to be suppressed.

Combining Images

As well as providing the facility to process more than one video stream at a time, the OSVP also includes a Combiner block that can be instantiated to pull the output from OSVP video channels together into a single final image. The Combiner allows up to 16 channels to be combined into a single video frame, with the user specifying the X,Y position and the transparency of that image and which layer it occupies.

In particular, it removes the need to write any Kernel Mode code and allows the same source code to be used across compatible but distinct implementations of any system.

Additional Technical Details

Frame Synchronisation

Differences between the input and output frame rate are handled by Frame Sync logic within the OSVP core that repeats frames or drop frames as required.

Producing Interlaced Output

To allow video to be output in Interlaced formats, the OSVP suite also includes an Interlacer block that can be instantiated alongside the OSVP core where Interlaced output is required.

Interfacing to Other IP

The OSVP core and other blocks of the OSVP Suite all offer AXI4 interfacing: AXI4-S stream interfacing for video, AXI4-Lite interfacing for control and

Software Support

The OSVP Suite IP includes drivers, kernel mode code and other supporting software that allow the development of applications within OmniTek's FPGA Software Interface Framework, which has been specifically developed to make prototyping easy by offering the same API for accessing FPGA IP facilities across different operating systems (Linux or Xilkernel or Windows{???}) and different hardware implementations.

AXI4-MM for memory management. These interfaces are supported as standard on Xilinx FPGA IP, making the blocks easy to integrate with other IP for Xilinx FPGAs. The blocks are also supplied ready for integration with Xilinx's Vivado IPI Design Environment.

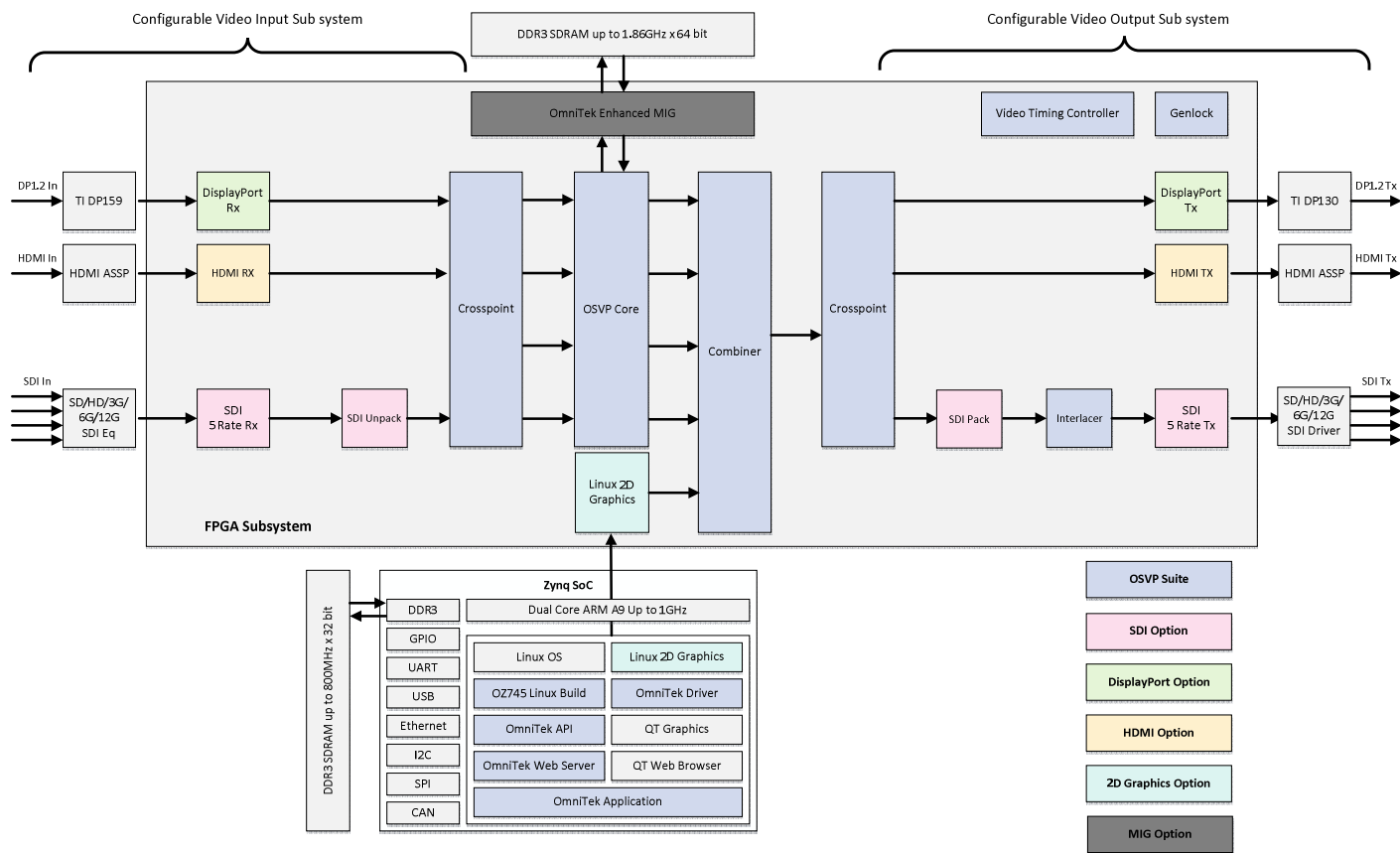
SDRAM Handling

Operations such as resizing and deinterlacing involve reading and writing to SDRAM. Processing multiple channels therefore requires multiple SDRAM accesses, together with the necessary logic to arbitrate the different operations. This logic is built into the OSVP core and is presented as a single AXI4-MM interface to the Xilinx MIG that provides the I/O services.

Reference Designs

OmniTek has developed a range of reference designs for the OSVP Suite, demonstrating how the cores can be used to provide particular functions and how to make the best use of the available bandwidth. Licensed versions of OSVP can be tailored to include the reference design that best matches the customer's needs.

The diagram below illustrates the OZ745 OSVP Reference design which runs under Linux and makes use of the Zynq ARM CPU on OmniTek's OZ745 Video Development kit, shown {{somewhere: currently below}} together with an FMC that adds two 6G-SDI inputs, two 6G-SDI outputs and a DisplayPort 1.2 port.

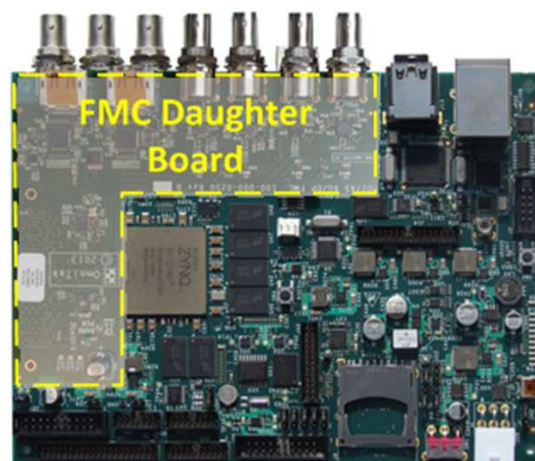


OZ745 OSVP Reference Design

The OSVP core is the processing engine at the heart of a number of Xilinx RTVE Real-Time Video Engine designs. These designs integrate the IP blocks of the OSVP Suite with Xilinx connectivity IP to create a complete working FPGA design that can be used both to evaluate the performance of the IP blocks in a video application and as a starting point for your own video system designs.

The reference designs comprise firmware, one or more applications and the drivers needed to control the design, all designed to work within the framework of OmniTek's FPGA Software Interface. The benefit of this interface is that it has been specifically developed to make evaluation and prototyping easy by allowing the same application to run on different system implementations. In the Evaluation version of the design this application is pre-compiled but, in Licensed versions, it is available as source code. A UI is generated by a web server for remote control.

Designs are built using Vivado IPI and integrate with the Xilinx AXI interconnect and the Xilinx AXI-MIG SDRAM controller. All IP block interconnect signals use AXI4 interconnect bus protocols.



OmniTek OZ745 Video Development Kit, with FMC daughter card that adds 2x 6G SDI inputs, 2 x 6G SDI outputs (both up to 4K), DisplayPort 1.2 input and output

Example IP Core Resource Use

	LUTs	Registers	RAMB36 Memory Blocks	DSPs
Chroma Resampler	600	822	0	24
Deinterlacer	7893	8769	40	14
Colour Space Converter	251	392	0	18
Noise Reduction	1356	3462	7	0
Cropper	451	1273	0	0
Resizer	2977	5101	32	54
1 4K60 Channel Total	14750	22619	76	110
Combiner	3346	4326	0	36
Interlacer	59	158	2	0
OZ745 OSVP Reference				
Design Total	162995	225798	355	510

Reference Design Availability

The OZ745 OSVP Reference is not the only OSVP reference design available from Omnitek. Other design covering a range of devices and operating systems are available and Omnitek can advise on the best one to suit your needs.

Device	Zynq 7	Kintex 7	UltraScale Kintex
Hardware Platform	OZ745	KC705	KCU105
Features			
4K	✓		
8K			✓
120Hz		✓	
Genlock	✓		
Connectivity			
SDI SD to 3G	✓		
SDI 6G to 12G	✓		✓
Quad 12G SDI (8K)			✓
HDMI 1.4 Rx	✓	✓	
HDMI 1.4 Tx	✓	✓	
DisplayPort 1.2 Tx	✓	✓	
CPU			
ARM	✓		
Microbase		✓	✓
OS			
Linux	✓		
XilKernal		✓	✓

Product Options

OSVP Suite: OSVP core offering 1– 8 channels of up to 1080p resolution. Comprises 4:2:2 to 4:4:4 Chroma resampler, colour matrix, de-interlacer, crop, re-size and frame synchronization. Also includes the Combiner and Interlacer.

OSVP Advanced Option: Adds support for up to two channels of 4K Ultra HD. Also adds 6-axis colour correction, noise reduction, super-resolution image enhancement, enhanced cadence detection and low-angle de-interlacing.

OSVP 120Hz Option: Adds support for output frame rates up to 120Hz.

Resampler Option: Adds 4:2:2 to 4:2:0 and 4:2:0 to 4:2:2 resamplers.

2D Graphics Option: Adds an OS framebuffer and 2D acceleration.

SDI Option: Adds SDI I/O connectivity.

HDMI Option: Adds HDMI I/O connectivity.

DisplayPort Option: Adds DisplayPort I/O connectivity.

Enhanced MIG Option: Enhances the MIG enabling higher efficiency when using OSVP.

8K Option: coming soon!

License Levels

Evaluation: Compiled software and firmware for running on an OZ745, KC705 or KCU105 board.

Extended Evaluation: Encrypted firmware source with timeout. Full source of Reference Design project and software.

Full License: Encrypted firmware source. Full source of Reference Design project and software.

Source License: Unencrypted Firmware source. Full source of Reference Design project and software.

Consultancy

Omnitek also offers core design consultancy services and a range of related cores such as PCIe video capture and playback



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