VIVADO IP INTEGRATOR: ACCELERATED TIME TO IP CREATION AND INTEGRATION

Accelerating the development of smarter systems requires levels of automation that go beyond RTL-level design. With the introduction of the Vivado™ Design Suite 2013.1, Xilinx delivers a SoC-strength, IP- and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation.

Vivado Design Suite dramatically accelerates product development cycles by enabling designs to be created more easily, meet timing more quickly, and by automating — not dictating — the developer's preferred design flow. Vivado Design Suite is built on a revolutionary, shared, scalable data model co-optimized for Xilinx® All Programmable FPGAs, SoCs, and 3D ICs. Accelerated design integration is achieved through a new IP-centric design flow that quickly turns a user's design or algorithms into reusable IP.

The Vivado Design Suite 2013.1 release includes the IP Integrator (IPI) feature, a new IP-centric design flow for accelerating the time-to-system integration. IPI increases programmable design productivity by 4X, lowering design costs and accelerating development of smarter systems.

Accelerated Intelligent IP Integration

To accelerate the creation of highly integrated, complex designs in All Programmable devices, Vivado Design Suite 2013.1 is delivering intelligent IP integration with an early access release of the new IPI feature, which provides a new graphical and Tcl-based, correct-by-construction, IP- and system-centric design development flow.

Built on the foundation of the Vivado integrated design environment, the IPI feature provides a device and platform aware, interactive environment that supports intelligent auto-connection of key IP interfaces, one-click IP subsystem generation, real-time DRCs, and interface change propagation, combined with a powerful debug capability.

With IPI, design is correct-by-construction. Working at the interface level, design teams can rapidly assemble complex systems and leverage Vivado tools to ensure that designs and IP are configured correctly. IPI's built-in automated interface, device driver, and address map generation accelerates design assembly. Getting from concept to debug has never been faster.

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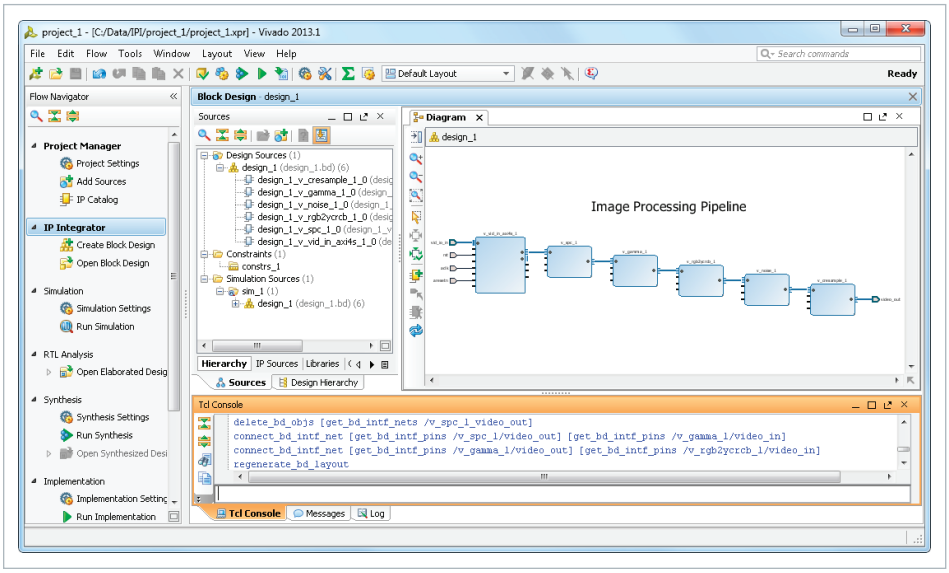
VIVADO DESIGN SUITE WITH IP INTEGRATOR



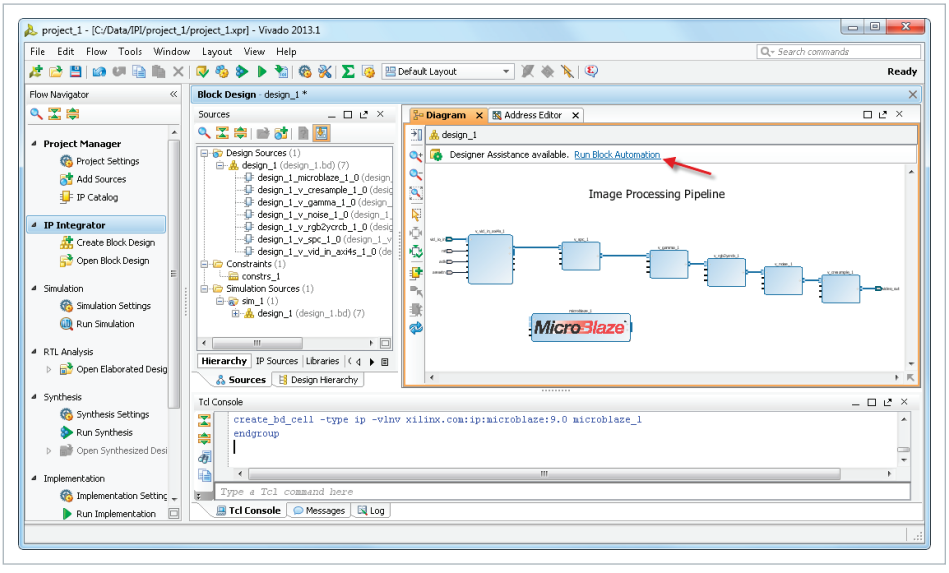
Vivado Design Suite provides an extensible IP catalog, which can contain Xilinx, third-party, and intra-company IP that can be shared across a design team, division, or company. Vivado Design Suite leverages industry standards such as ARM®'s AXI interconnect and IP-XACT metadata when packaging IP. Now with IPI, Vivado Design Suite facilitates rapid development of smarter systems, which can include embedded, DSP, video, analog, networking, interface, building block, and connectivity IP consolidated into a hierarchical system and IP-centric view.

With open, industry IP standards, Vivado Design Suite enables third-party vendors to deliver their IP portfolios to developers, who can now integrate them with Vivado IPI. Users can also package their own RTL, or C/C++/SystemC and MATLAB®/Simulink® algorithms into the IP catalog using Vivado High-Level Synthesis (HLS) or System Generator for DSP with the Vivado IP packager. Leveraging the extensible IP catalog, IPI provides automated IP subsystem generation. As an example, to generate a MicroBlaze™ subsystem, a designer selects the MicroBlaze core, adds it to the design, and then uses IPI's built-in block generation feature and one-click IP customization to rapidly configure the interconnect, peripherals, memory map, and device driver information to increase designer productivity.

Co-optimized for Xilinx All Programmable Solutions

Since its inception, Vivado Design Suite, with its analytical place and route technology that concurrently optimizes for congestion, wire length, and timing, has been architected to be device aware and co-optimized for maximum utilization of Xilinx's All Programmable solutions. However, now Vivado is not only device aware—it is target platform aware—supporting all Zynq™ All Programmable SoCs (AP SoC) and 7 series FPGA boards and kits. By being target platform aware, Vivado Design Suite now configures and applies board-specific design rule checks, which ensures rapid bring up of working systems.

MICROBLAZE IP ONE-CLICK SUBSYSTEM GENERATION



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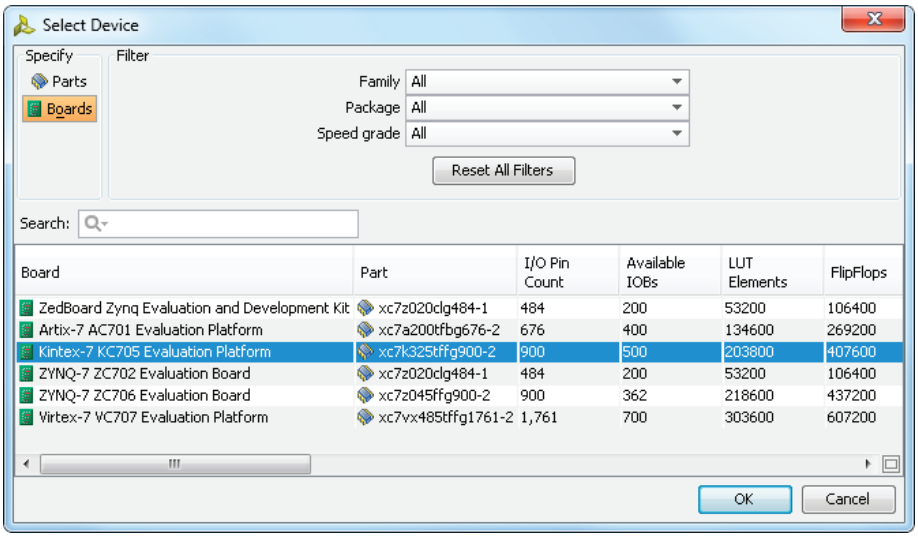
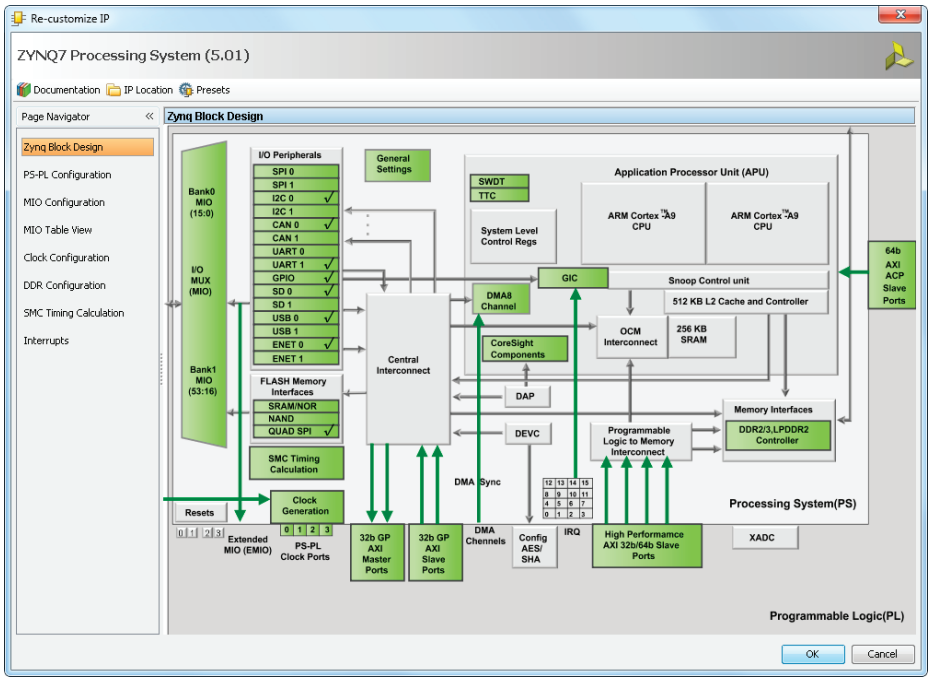
TARGET PLATFORM AWARE: CONFIGURES AND APPLIES BOARD-SPECIFIC DESIGN RULE CHECKS



For example, by selecting the Zynq-7000 AP SoC ZC702 Evaluation Kit, and instantiating a Zynq processing system within IPI, Vivado Design Suite preconfigures the processing system with the correct peripherals, drivers, and memory map to support the board. Embedded design teams can now more rapidly identify, reuse, and integrate both software and hardware IP, targeting the dual-core ARM processing system and high-performance FPGA logic.

The user easily specifies the interface between the processing system and their logic with a series of dialog boxes. Interfaces are automatically generated, optimized for performance or area, and then users can add their own custom logic or use the Vivado IP catalog to complete their design.

PRECONFIGURED PROCESSING SYSTEM FOR ZYNQ AP SOC ZC702 EVALUATION KIT



Summary

Rapid development of smarter systems requires levels of automation that go beyond RTL-level design. Vivado Design Suite is uniquely positioned to do this. The Vivado IP Integrator accelerates IP- and system-centric design implementation by providing the following:

Tight integration within the Vivado Integrated Design Environment

- Seamless inclusion of IPI subsystems into the overall design
- Rapid capture and packing of IPI designs for reuse
- Tcl scripting and graphical design
- Rapid simulation and cross-probing between multiple design views

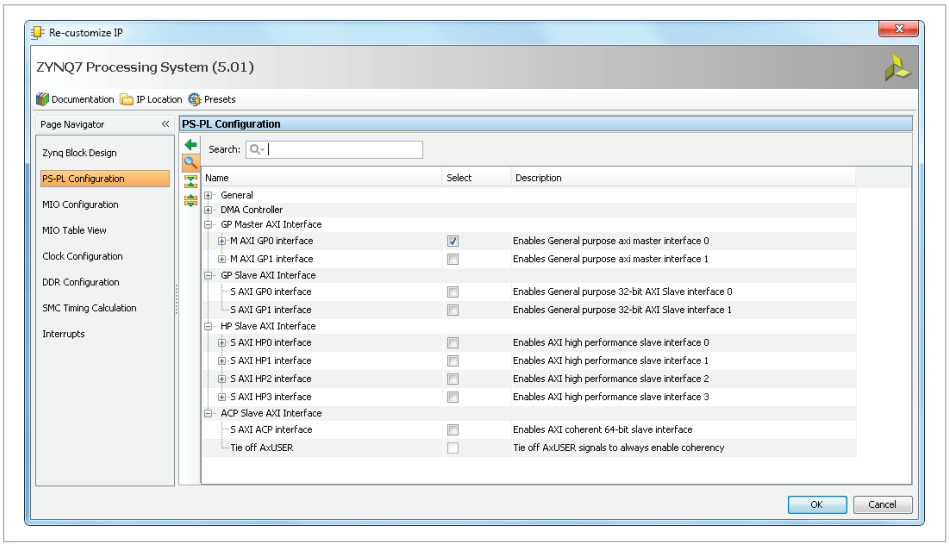
Support for All Design Domains

- Support for processor or processor-less designs
- Integration of algorithmic (Vivado HLS and System Generator) and RTL-level IP
- Combination of DSP, video, analog, embedded, connectivity and logic

Hierarchy Support

- Matches typical designer flows
- Easy to reuse complex subsystems

AUTOMATED INTERFACE GENERATION



Advanced Design Services

- DRCs on complex interface level connections during design assembly
- Recognition and correction of common design errors
- Automatic IP parameter propagation to interconnected IP
- System-level optimizations

Take the NEXT STEP

To learn more about the Vivado Design Suite featuring the IP Integrator, please visit **www.xilinx.com/vivado**

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