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# LVDS Source Synchronous DDR Deserialization (up to 1,600 Mb/s)

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## Summary

Xilinx 7 series FPGAs contain input SerDes (ISERDES) primitives that make the design of deserializer circuits very straightforward and allow operation at speeds up to 1,600 Mb/s per channel, when using per-bit deskew, depending on the family and speed grade used. This application note describes how to use ISERDES efficiently for reception of 1 to n data that is using a forwarded edge-aligned DDR clock and low-voltage differential signaling (LVDS) for data transmission.

Download the Reference Design Files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design Files, page 9.

## Introduction

This type of 1 to 4 interface using DDR clocking is shown in Figure 1. The macros supplied with this application note cover serdes ratios of 1:4, 1:6, and 1:8 and a somewhat modified version is available to cover 1:10.

The macros are parameterizable for the number of LVDS data lines received per clock line. All data bits in a channel should be placed into a single I/O bank of a 7 series device, and the input clock signal pair should be placed on clock-capable I/O pins.

Incoming data is deskewed, that is, any skew caused by VT variations, as well as PCB and package skew is removed in real time on a per-pin basis using the input delays (IODELAYE2) present in the 7 series FPGAs. This allows you to relax the PCB routing skew requirements and provides tighter timing margins. Real-time deskew uses a separate state machine per pin, and this does require transitions on a data line to function correctly. The state machine also provides the possibility of generating chipscope-viewable eye opening data on a per-line basis.

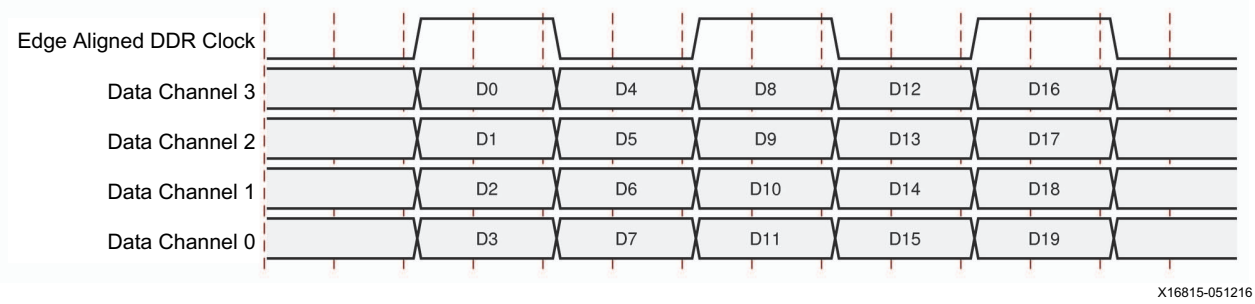


*Figure 1:* **4-bit Data Stream with DDR Clock and 1:4 Data Formatting**

# ISERDES Guidelines

The 7 series FPGAs have high-range (HR) and high-performance (HP) I/O banks. Each I/O bank provides 50 I/O of which two are always single ended and 48 can be used as single ended or differential I/O. As shown in Figure 2, eight single ended/four differential I/O can be used as clock inputs. Each single ended I/O can be connected to dedicated serializer (OSERDES) and/or deserializer (ISERDES) primitives available in both HR and HP banks.

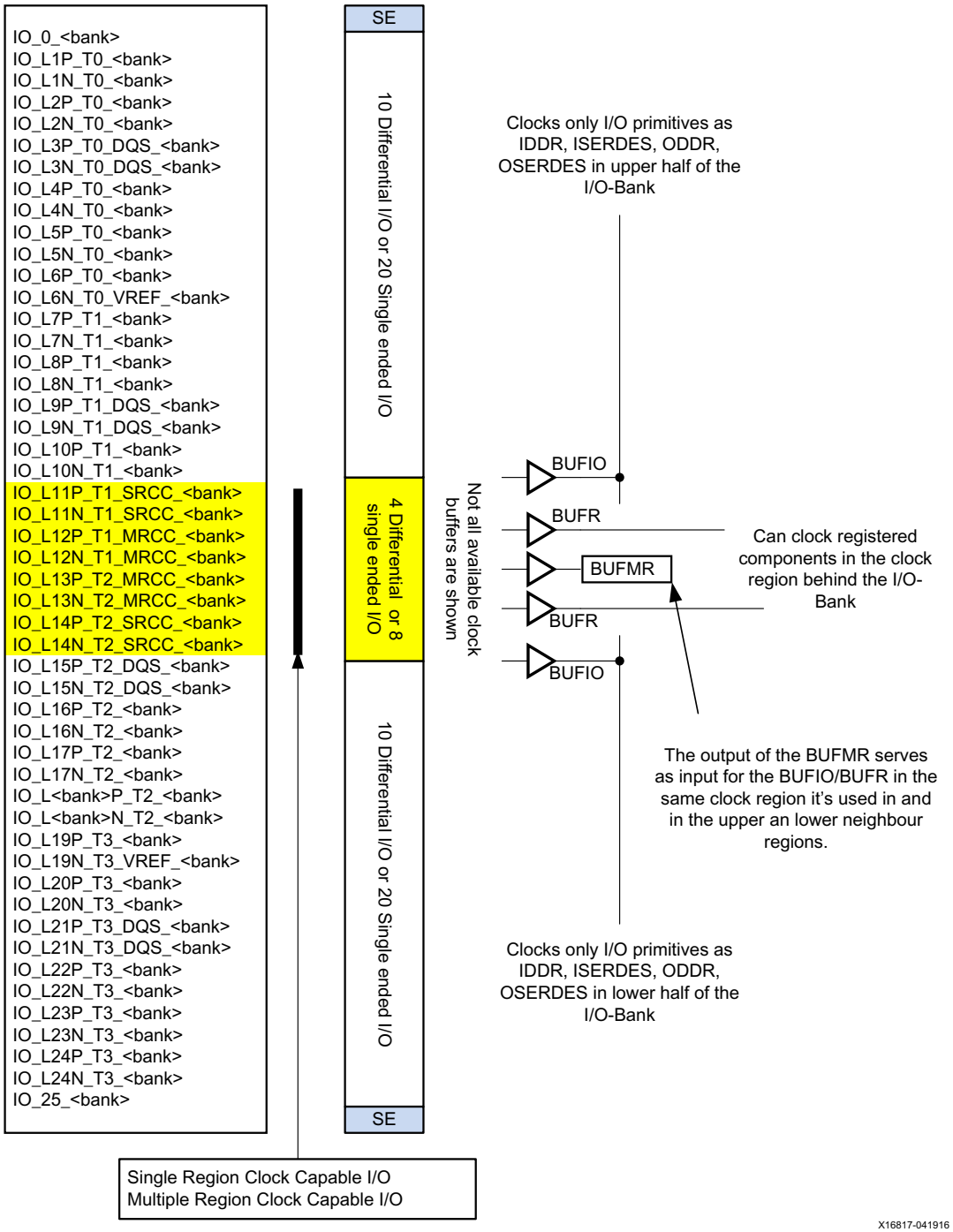


*Figure 2:* **I/O Bank and Clocking Details**

The focus for the application note are the ISERDESE2 (Figure 3) and IDELAYE2 (Figure 4) primitives. The ISERDESE2 from two adjacent blocks (master and slave) that can be cascaded to give a 10-bit or 14-bit block. This gives the possibility of ISERDES input ratios from 1:2, 1:4, 1:6, 1:8, 1:10 and 1:14 for double data rate (DDR) operation.

Cascading the ISERDESE2 blocks is not a problem when differential signaling standard is used, as these standards use both I/O logic tiles (master and slave) associated with the ISERDESE2 components, thus using two cascaded ISERDES is effectively free.

The HR I/O banks support LVDS 2.5V I/O and HP banks support LVDS at 1.8V ($V_{CCO}$ level). For details about these HR and HP I/O banks and the ISERDESE2 and IDELAYE2 components, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 1].

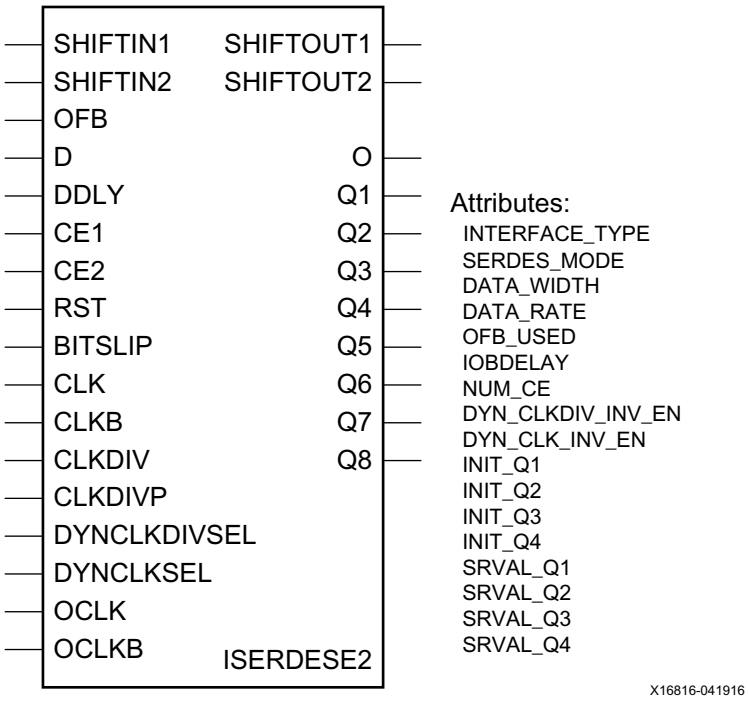


*Figure 3:* **ISERDESE2 Primitives**

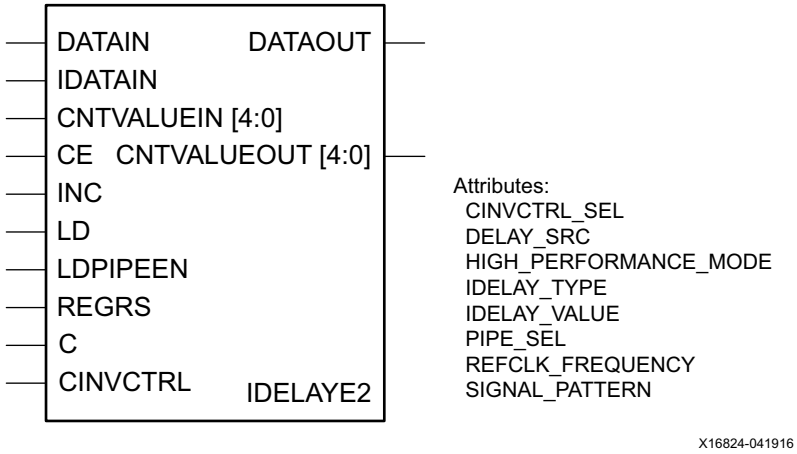


*Figure 4:* **IDELAYE2 Primitives**

# Clocking Guidelines

The discussed designs use BUFIO and BUFR clocking within a single clock region, further use of more than one clock region will require a domain transfer from the BUFR clock network to a global clock network, or alternatively the BUFMR clock buffer present in the 7 series can be used to enable BUFRs in three vertically adjacent regions to be used, see the *7 Series FPGAs Clocking Resources User Guide* (UG472) [Ref 2] from page 102 on for more information. Global clock and PLL/MMCM specification for 7 series FPGAs are given Table 1. The BUFIO, BUFR and BUFMR setup in a 7 Series I/O bank is shown in Figure 2, page 2.

*Table 1:* **Global Clock and PLL/MMCM Specifications in 7 Series FPGAs**

| FPGA | Speed Grade | I/O Clock Network Maximum (BUFIO) | Regional Clock Network Maximum (BUFR) |
|---|---|---|---|
| Artix™-7 | -1 | 600 MHz | 315 MHz |
| Artix-7 | -2 | 680 MHz | 375 MHz |
| Artix-7 | -3 | 680 MHz | 420 MHz |
| Kintex™-7 | -1 | 710 MHz | 450 MHz |
| Kintex-7 | -2 | 800 MHz | 540 MHz |
| Virtex®-7 | -1 | 710 MHz | 450 MHz |
| Virtex-7 | -2 | 800 MHz | 540 MHz |
| Virtex-7 | -3 | 800 MHz | 600 MHz |

# Introduction to Deserialization and Data Reception

## Clock Reception

The topology for this mechanism is very straight forward. The received DDR clock is routed from a clock-capable input pin-pair (differential) or pin (single ended) without using an input delay, to both a BUFIO and a BUFR in the clock region. The BUFR is configured as divide by n, where n is half the required serial-to-parallel rate. The BUFIO clock is used to sample the receiver data in the input ISERDESE2, while the BUFR is used to clock parallel data out of the input ISERDESE2 and clock the controlling state machines. The output of the BUFR is also used to clock the user logic. The incoming clock signal is also routed through an input delay element (IDELAYE2) and on to an input serial-to-parallel primitive (ISERDSE2). The data from the serial-to-parallel primitive is only used internally to the macro for initial training purposes.

Following a power-up or reset the initial calibration state machine uses the incoming clock as a training signal to determine the initial delay setting required by the data bit receivers. This behavior requires no particular pattern on the data lines and can be static if necessary, only the incoming clock is used to determine the initial calibration. The clock receiver is shown in the upper portion of Figure 5.

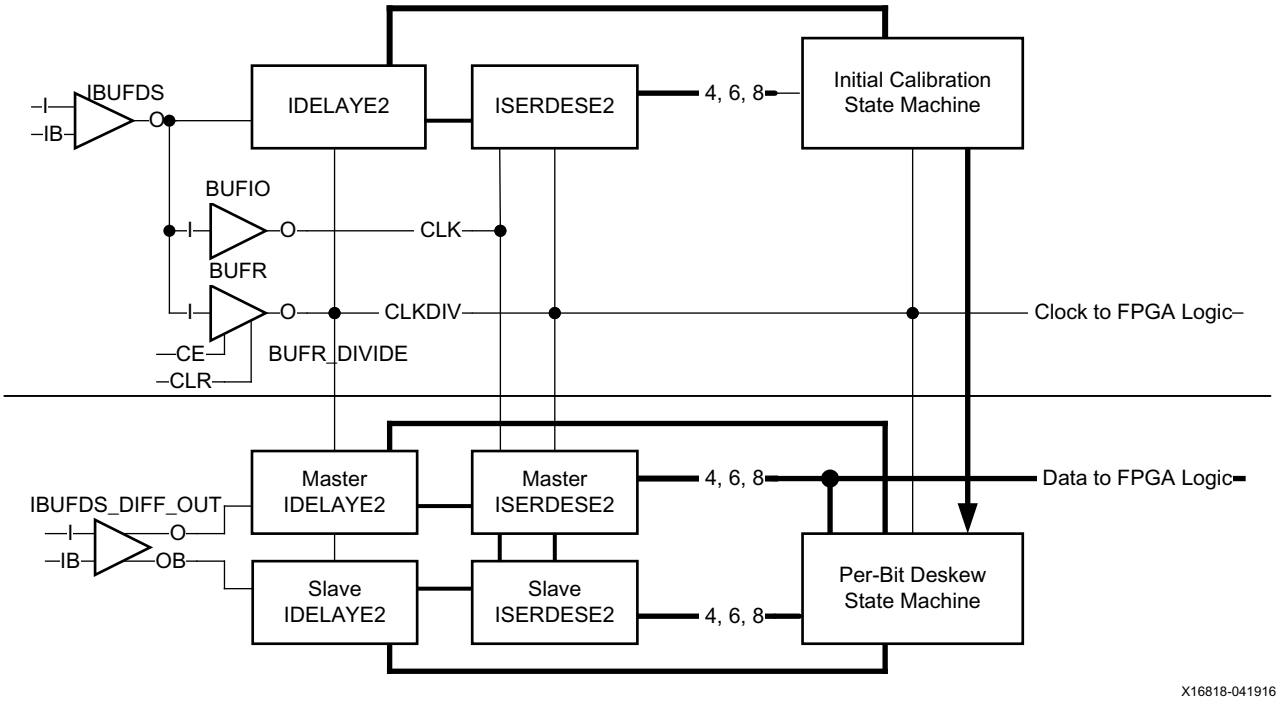


*Figure 5:* **Clock and Data Receiver Logic**

## Data Reception and Per-Bit Deskew

As shown in the lower portion of Figure 5, the incoming LVDS data lines are routed to both a master and slave input delay via the IBUFDS_DIFF_OUT input buffer, and then routed to the master and slave ISERDESE2. Parallel data from the master ISERDESE2 is forwarded into the user logic and also into the controlling state machine. Parallel data from the slave ISERDESE2 is only used by the controlling state machine.

The initial data delay is determined as described in the preceding Clock Reception section, and is passed to the IODELAYE2s on the data lines. This ensures that the delays are positioned in the correct place immediately, and that the per-bit deskew algorithm is only used to fine-tune each data line from that point on.

The initial delay of the master data delay is set to be nominally in the middle of the eye. The slave delay is set to be a half-bit period different (earlier or later). As a result, two samples are taken of the incoming data line, separated by a half-bit period. To work out how many taps there are in a half-bit-time, the macros have a a 16-bit input data bus that allows you to specify the bit rate directly via a 16-bit hexadecimal constant. For example, 622 Mb/s should be specified with a constant of `216'h062` (X"0622" in VHDL).

The algorithm used to then determine the correct sampling delay works as follows. If the two samples taken are half a bit period apart (following a transition) and are the same, then the sampling point is too late and the input delays need to be reduced by one tap (Figure 6). If the two samples taken (following a transition) are different, then the sampling point is too early and the input delays need to be increased by one tap (Figure 7). This mechanism requires changes in the incoming data. If the data line is a static-zero or static-one the delays remain at their initial value. Because it is impossible to do this comparison in real time synchronous to the sampling clock, the parallel received data is used, that is, two 4, 6 or 8-bit samples per input line are required.

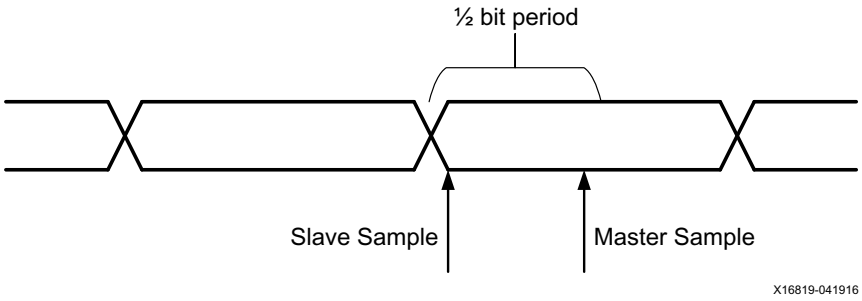


*Figure 6:* **Data Sampling Delay Too Long**

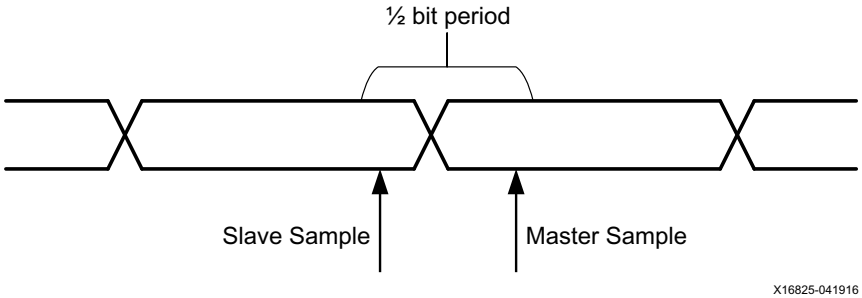


*Figure 7:* **Data Sampling Delay Too Short**

There are two pathological cases possible with this algorithm: One is when a master delay wraps around towards zero and the other when the master delay wraps around away from zero. In either case data corruption occurs, with either a bit being received twice, or not at all. The logic includes registers and multiplexers to detect either situation and inserts pipeline stages appropriately to ensure that data corruption never occurs following either event.

The disadvantage is that this approach requires an amount of logic to implement, the advantage is that each input line is individually deskewed in real time, while correct data reception is guaranteed. This allows sources of skew such as PCB routing, pin delays, and transmitter pin variation to be removed from the timing analysis.

The deskew algorithm works with any amount of bit variation in either direction, but it is recommended that the input and clock line skew is kept within plus or minus one-fourth UI. The circuit still works outside this range, but further user logic might be required to perform word deskew.

## 1-to-10 Data Reception

The diagram for 1:10 data reception is shown in Figure 8. The receiver basically uses a 1:4 receiver as already described (BUFR 'A' configured as divide-by-2). The output of this receiver is then applied to a distributed RAM-based gearbox for translation. Another clock is also required and this is generated by a second BUFR (B) which is configured to divide-by-5. The 4-bit words applied at the BUFR 'A' clock rate are converted to 10-bit reads which are output from the gearbox at the BUFR 'B' clock rate. The timing diagram for this gearbox feature is shown in Figure 9.

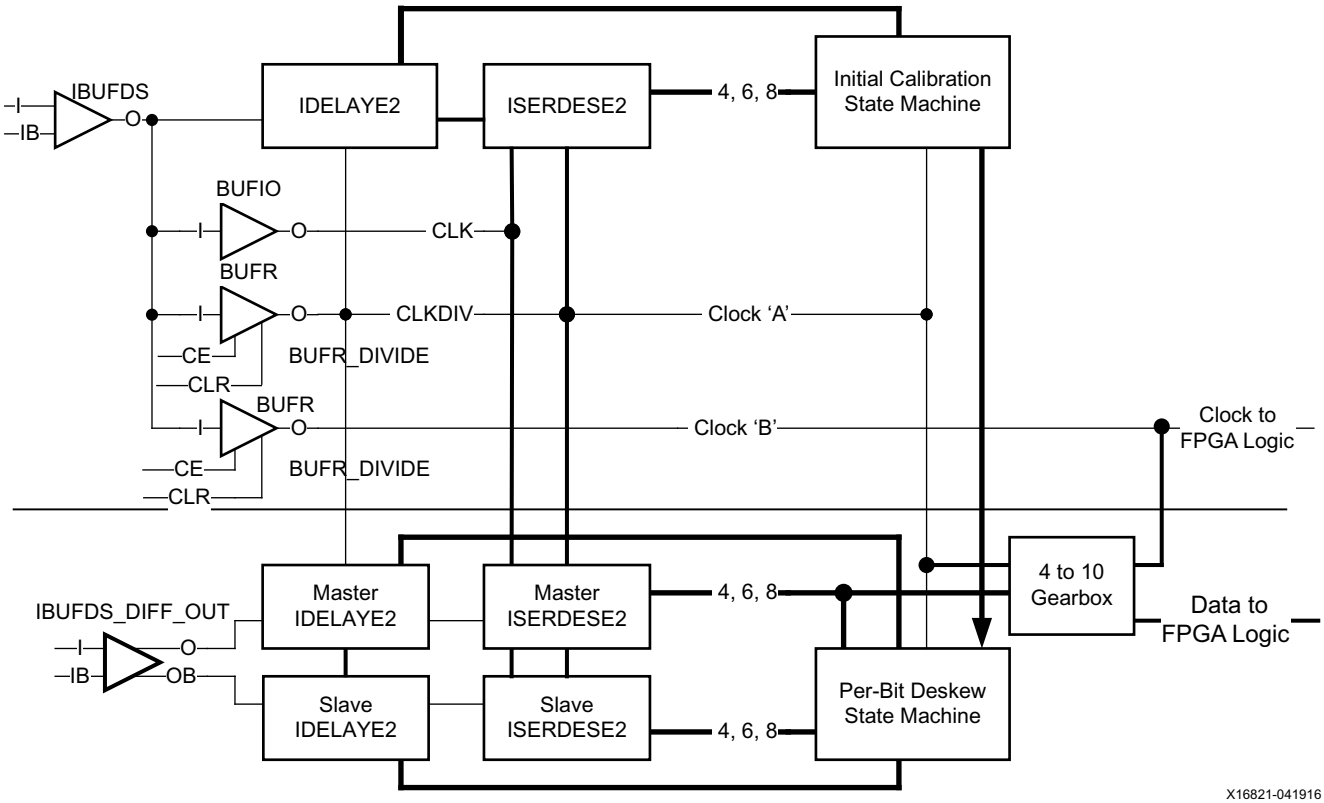


*Figure 8:* **Clock and Data Receiver Logic**

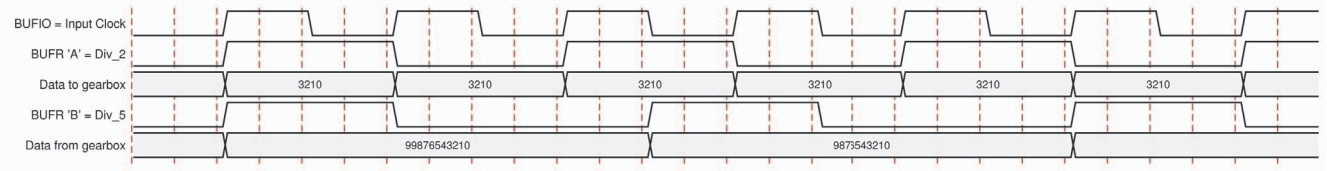


*Figure 9:* **4-bit to 10-bit Gearbox Waveform**

## Minimum Data Rate Considerations

The data capture mechanism is dependent on the IODELAYE2 block. The IDELAYE2 has 32 delays of nominally 78 ps when the IDELAYCTRL clock is set to 200 MHz. The minimum capture frequency = 78 x 32 = 2,496 ps = ~400 Mb/s. When the IDELAYCTRL primitive clock is set to be 300 MHz the tap delay decreases to 56 ps improving the receiver margin but increasing the minimum capture frequency up to ~550 MHz. Any bit rate under these values could result in the situation where there are no edges at all being captured in the delay line at any one time. This causes the initial clock calibration to fail (the circuit loops continuously). Data reception below 400 Mb/s therefore takes a best-guess approach to training. If an edge is found in the delay line, then the initial delay is set to this value, ± 10 hex taps. If no edge is found, then the delay line is set to be 10 hex taps. In either case, the delay is set to be at least 10 hex taps away from either edge of the eye, which is acceptable at these lower bit rates.

## Receiver Timing Considerations

Several sources of uncertainty need to be taken into account for the receiver. These sources should be subtracted from the bit period to analyze whether the design meets your requirements. To aid in this, an Excel spreadsheet is included with the design ZIP file to allow rapid analysis. A screen capture is shown in Figure 10.

| | | | |
|---|---|---|---|
| **Receiver Margin Calculations** | | | |
| **Version 1.1** | | | |
| | | | |
| Bit Period | **1000** | ps | User required bit period |
| Design Mode | DDR | | |
| Delay Reference Clock | **200** | MHz | User selectable |
| IO Delay HIGH PERFORMANCE MODE | **TRUE** | (TRUE/FALSE) | User selectable |
| Sample Clock | BUFIO | | |
| | | | |
| MAX number of taps used (decimal) | 13 | | |
| | | | |
| Uncertainties when using per-bit deskew | | | |
| | | | |
| Per bit deskew accuracy | 156 | ps | Plus or Minus two delay line taps (including delay rounding) |
| Pattern Dependent Jitter in Delay line | 64 | ps | 9 ps per tap default or 5 ps per tap in HIGH PERFORMANCE MODE |
| Sampling Clock Duty Cycle Distortion | 60 | ps | (Half of any fixed duty cycle distortion will removed by the per-bit deskew logic) |
| Transmitter jitter and ISI | **120** | ps | Any PCB and package data skew will be removed by the per-bit deskew logic |
| | | | |
| Remaining Window after Receiver Uncertainties | 600 | ps | |

X16823-041916

*Figure 10:* **Receiver Margin Calculator**

## Eye Monitoring

A close to real time eye monitoring circuit has been added to the macros in the reference design.

# Reference Design Files

You can download the Reference Design Files for this application note from the Xilinx® website. The reference design files are available in both Verilog and VHDL.

The name of the appropriate file is included in the figures for different methodologies shown throughout this document. Also included are example top-level files and example timing constraints for both the ISE® and Vivado® design suites.

Each of the DDR data input modules is parameterizable for input width (number of input pins per interface). The files included are:

- serdes_1_to_468_idelay_ddr.v/vhd
- serdes_1_to_10_idelay_ddr.v/vhd

Table 2 shows the reference design matrix. Table 3 shows device utilization.

*Table 2:* **Reference Design Matrix**

| Parameter | Description |
|---|---|
| **General** | |
| Developer Name | Xilinx |
| Target Devices | 7 Series FPGAs |
| Source code provided | Yes |
| Source code format | Verilog and VHDL |
| Design uses code and IP from existing Xilinx Application note and reference designs, CORE Generator software, or third party | No |
| **Simulation** | |
| Functional Simulation Performed | Yes |
| Timing simulation performed | No |
| Test bench used for functional and timing simulations | Yes |
| Test bench format | Verilog and VHDL |
| Simulator software/version used | ISIM |
| SPICE/IBIS simulations | No |
| **Implementation** | |
| Synthesis software tools/version used | Vivado tools 2016.1 or later |
| Implementation software tools/versions used | Vivado tools 2016.1 |
| Static timing analysis performed | Yes |

*Table 2:* **Reference Design Matrix *(Cont'd)***

| Parameter | Description |
|---|---|
| **Hardware Verification** | |
| Hardware verified | Yes |
| Hardware platform used for verification | KC705 and/or VC707 with FMC 107 |

*Table 3:* **Device Utilization**

| Design File | Clock Buffers | Slices | ISERDES |
|---|---|---|---|
| `serdes_1_to_468_idelay_ddr.v/vhd`<br>Per-bit deskew enabled | 2 | ~8 per line | 2 per line |
| `serdes_1_to_10_idelay_ddr.v/vhd`<br>Per-bit deskew enabled | 3 | ~17 per line | 2 per line |
| `serdes_1_to_468_idelay_ddr.v/vhd`<br>Per-bit deskew and monitoring enabled | 2 | ~36 per line | 2 per line |
| `serdes_1_to_10_idelay_ddr.v/vhd`<br>Per-bit deskew and monitoring enabled | 3 | ~45 per line | 2 per line |

# Conclusion

The 7 series FPGAs perform in a wide variety of applications requiring serialization and deserialization factors of 4, 6, 8, or 10-to-1 at speeds from 400 Mb/s to 1,600 Mb/s per channel with per-bit deskew enabled, depending on the 7 series family and speed grade used.

# References


1. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
2. *7 Series FPGAs Clocking resources User Guide* (UG472)
3. *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS181)
4. *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS182)
5. *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183)


# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 07/22/2016 | 1.0 | Initial Xilinx release |

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