XAPP1096 (v1.0.1) January 10, 2014

DC Coupling with 7 Series FPGAs GTX Transceivers

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Summary

This application note describes how the 7 series FPGAs GTX transceivers can be used for DC coupling applications.

Introduction

General transceiver usage in industry is AC-coupled links between the transmitter and receiver. The major drawbacks of AC-coupled links are:

- Discontinuities created by connections to the AC coupling capacitors.
- Routing congestion on boards due to AC coupling capacitors.
- Increase in board area due to AC capacitor placement.
- Loss of AC swing across the capacitor.
- Limitation on run length.
- Possible degradation of low-frequency signal content.

These drawbacks can be mitigated by using a DC link between the transmitter and receiver. One of the major drawbacks of using a DC link is the static/DC current.

7 Series FPGAs GTX Transceiver Capabilities

The 7 series FPGAs GTX transceivers can be used for DC-coupled links. The analysis of this application is divided into the following categories:

- Utilizing the GTX transceiver as a receiver.
- Utilizing the GTX transceiver as a transmitter.
- Communication between two GTX transceivers.

In an AC-coupled system for a typical current mode logic (CML) transceiver with on-die termination, the common mode at the RX input is dictated by the RX termination voltage. The common mode of the TX is dictated by the TX termination voltage and the output swing.

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Figure 1 shows a high-level diagram of an AC-coupled link.

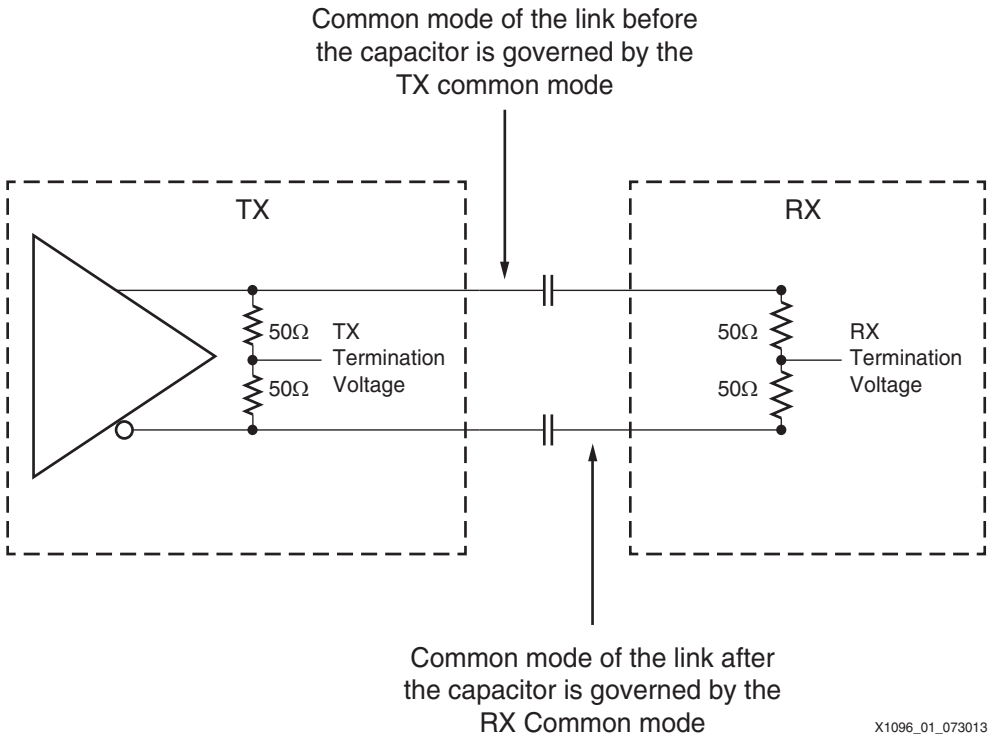

Figure 1: **High-Level Diagram of an AC-Coupled Link**

In a DC-coupled system, the common mode voltage of the link is typically determined by the TX termination voltage, the output swing, and the RX termination voltage.

Figure 2 shows a high-level diagram of a DC-coupled link.

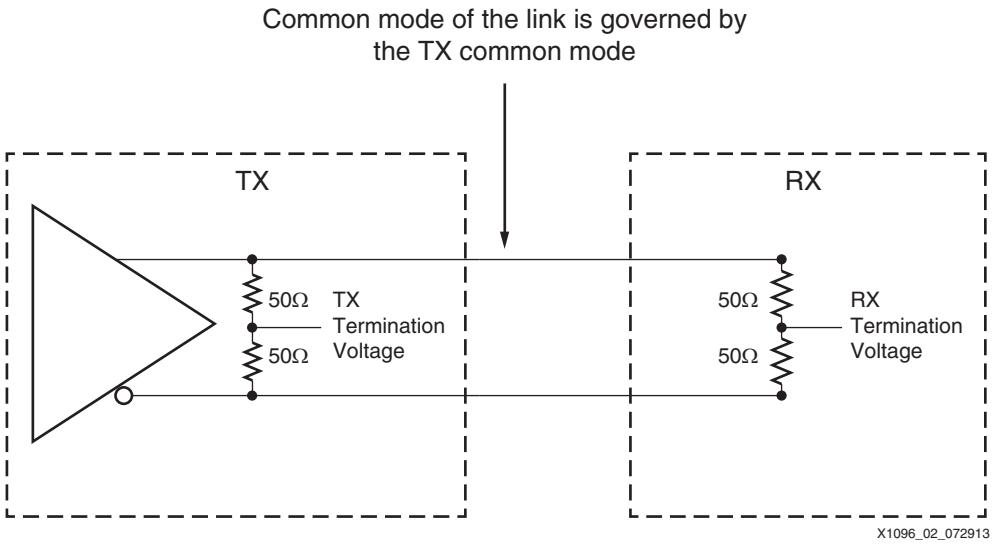

Figure 2: **High Level Diagram of a DC-Coupled Link**

Utilizing the GTX Transceiver as a Receiver

To use the Kintex®-7 FPGA transceiver as a DC-coupled receiver it is very important to analyze the line common mode of the system. The line common mode is a result of:

- TX termination voltage
- TX output swing
- RX termination voltage
- Biasing resistors (if applicable)

The RX can be terminated to either GROUND or AVTT to achieve the required line common mode voltage. The I_{DCIN} and I_{DCOUT} currents should be within the data sheet specifications (see *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* [Ref 1] and *Zynq-7000 All Programmable SoC (XC7Z030, XC7Z045, and XC7Z100): DC and AC Switching Characteristics* [Ref 2]).

The appropriate RX equalization mode (low-power mode (LPM) or decision feedback equalization (DFE)) should be selected based on these parameters:

- Operational frequency
- System loss
- Line common mode voltage

Recommended Settings

Depending on the line common mode voltage, the requirements for TX swing and RX equalization modes are shown in Table 1.

Table 1: **TX Swing and RX Equalization Requirements for GTX Receivers**

RX Equalizer Mode (1)(2)(3)	Line Common Mode (mV)	RX_CM_SEL [1:0]	PMA_RSVD2 [7:6]	Minimum Launch Amplitude (mVpp Differential)
DFE	700–1200	2'b00	2'b01	450
LPM	0–75	2'b01	2'b10	450
LPM	700–1200	2'b00	2'b01	150

Notes:

1. Refer to the *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* [Ref 1].
2. Refer to *Zynq-7000 All Programmable SoC (XC7Z030, XC7Z045, and XC7Z100): DC and AC Switching Characteristics* [Ref 2].
3. Refer to the *7 Series FPGAs GTX/GTH Transceivers User Guide* [Ref 3].
4. A 150 mV swing is used for very short reach only. Swings of 450 mV and higher are used for medium to long reach. Refer to the data sheets for the exact loss specifications for both DFE and LPM modes.

Table 2 specifies the maximum input swing at the RX pins.

Table 2: **Maximum Swing for Given Line Common Mode Voltage**

Line Common Mode Range (mV)	Maximum Input Swing (mVpp Differential)
0–75	1200
700–1100	2000
1100–1200	1200

Utilizing the GTX Transceiver as a Transmitter

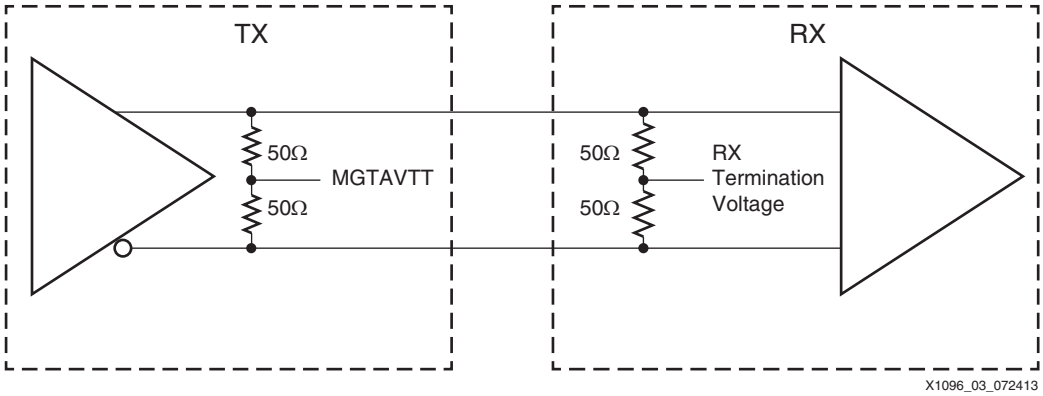

Figure 3: **High-Level Diagram of DC Link with GTX Transceiver as a TX**

The following guideline is recommended for using a GTX transmitter in a DC-coupled system:

- The I_{DCOUT}/I_{DCIN} maximum rating needs to be followed according to the data sheets [Ref 1] [Ref 2].

A quick reference table for I_{DCOUT} and I_{DCIN} can be found in Table 5.

Linking Two 7 Series FPGAs GTX Transceivers

A reliable DC link can be established between two GTX transceivers. The conditions in Table 3 should be met for a reliable DC-coupled link.

Table 3: **TX Swing and RX Equalization Requirements to Link Two GTX Transceivers**

RX Equalizer Mode	Line Common Mode (mV)	RX_CM_SEL [1:0]	PMA_RSVD2 [7:6]	Minimum Launch Amplitude (mVpp Differential)	Maximum Launch Amplitude
DFE	700–1200	2'b00 (AVTT)	2'b01	450	Refer to the data sheets(1)
LPM	700–1200	2'b00 (AVTT)	2'b01	150	

Notes:

1. Refer to the *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* [Ref 1] and *Zynq-7000 All Programmable SoC (XC7Z030, XC7Z045, and XC7Z100): DC and AC Switching Characteristics* [Ref 2].
2. Refer to the *7 Series FPGAs GTX/GTH Transceivers User Guide* [Ref 3].

Equation 1 can be used to determine the first order approximation of the line common mode voltage (AVTT Termination on RX). This equation applies to typical temperature and voltage conditions. The equation gives users a very basic approximation of the line common mode of the system.

$$\text{Voltage} = -0.021 \times (\text{TXDIFFCTRL_CODE}) + 1.1037 \qquad \textit{Equation 1}$$

Where:

Voltage = Line common mode voltage in volts

TXDIFFCTRL_CODE = Valid values [0...15]

Usage Examples

Example 1

Figure 4 shows an example termination.

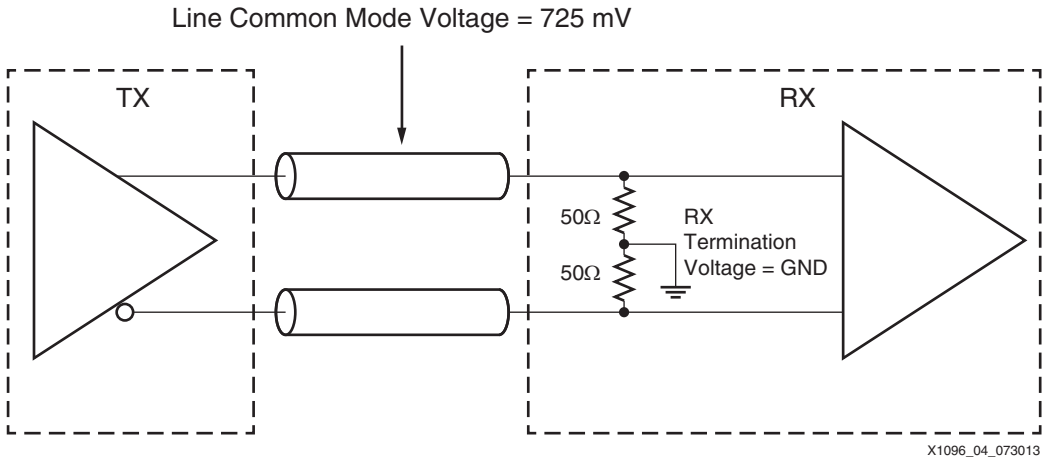

Figure 4: **Example 1**

In Figure 4:

- TX is a generic transmitter that can provide high termination voltage.
- RX is a very basic and high-level abstraction of the 7 series FPGA RX.

The assumption for this example is that the TX driver is able to provide a termination voltage such that the resultant line common mode voltage is 725 mV when the RX is ground terminated. With the data available, the common mode voltage of the line is 725 mV, which appears to be a viable scenario. Figure 4 can be modeled to a very simple circuit with a voltage source and resistor to ground, as shown in Figure 5.

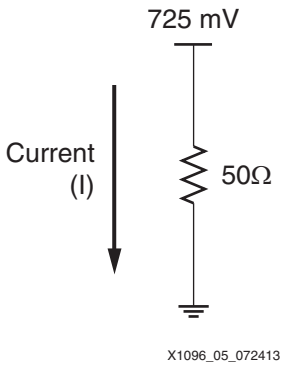

Figure 5: **Simplified View of Example 1**

Common mode voltage (V) = 725 mV

Resistance (R) = 50Ω

The current through the resistor can be calculated using Ohm's law (Equation 2):

$$I = \frac{V}{R} \qquad \textit{Equation 2}$$

$$I = \frac{725\ mV}{50\Omega} \qquad \textit{Equation 3}$$

$$I = 14.5\ mA \qquad \textit{Equation 4}$$

The 14.5 mA current is higher than the data sheet specification for $I_{DCIN} \leq 6.5$ mA for ground termination. The configuration shown in Figure 4 and Figure 5 is therefore invalid.

Example 2

This example is very similar to Example 1, but includes changes that make the configuration viable.

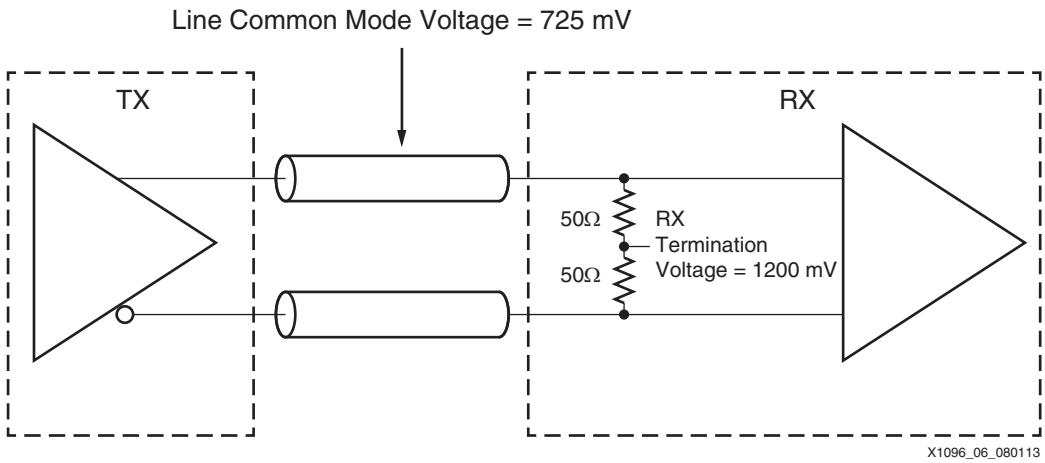

Figure 6: **Example 2**

In Figure 6:

- TX is a generic transmitter.
- RX is a very basic and high-level abstraction of the 7 series FPGA RX.

The assumption for this example is that the TX driver is able to provide termination voltage such that the resultant line common mode voltage is 725 mV when the RX is terminated to AVTT.

Figure 6 shows a simplified view of Example 2.

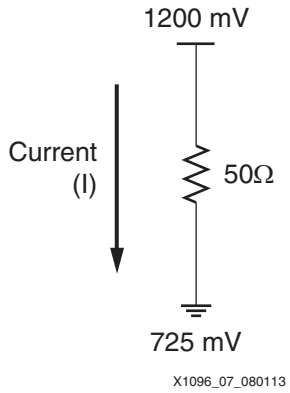

Figure 7: **Simplified View of Example 2**

The current through the resistor can be calculated using Ohm's law (Equation 5).

$$I = \frac{V2 - V1}{R} \quad \textit{Equation 5}$$

$$I = \frac{1200\ mV - 725\ mV}{50\Omega} \quad \textit{Equation 6}$$

$$I = 9.5\ mA \quad \textit{Equation 7}$$

In Equation 7, 9.5 mA is less than the I_{DCIN} current limit for AVTT termination. As shown in Example 1 and Example 2, it is imperative to meet all the conditions defined in these sections and in the data sheets in the DC coupling scenario. Failure to meet these conditions can result in physical damage to the device.

Example 3

GPON/GPON Like

A major application that uses DC-coupled links is Gigabit-capable Passive Optical Networks (GPON). This section discusses a numerical example for a GPON-like application (Figure 8).

Note: For more information, refer to *Introduction to LVDS, PECL and CML (Maxim Integrated)* [Ref 4], *Interfacing between LVPECL, LVDS and CML* [Ref 5], and *Interfacing between LVPECL, VML, CML and LVDS Levels* [Ref 6].

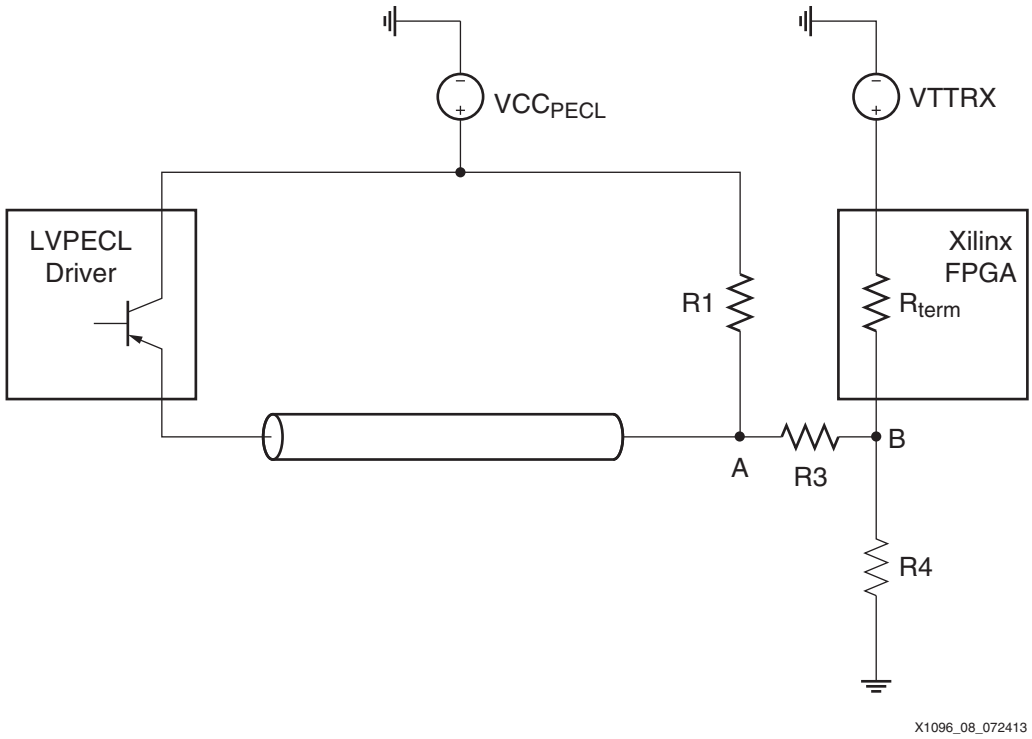

Figure 8: **GPON Network**

There are four considerations for interfacing the GTX receiver to an LVPECL driver:

- Open circuit Z_{IN} at A = 50Ω
- Open circuit Thevenin voltage (OCT V) = 1.3V = V_A

  Note: The value was provided by the LVPECL vendor. This condition is true when the TX driver is not present and only a VCC_{PECL} supply is present.
- Common mode requirements:
  - $V_{CM\text{-}PECL}$ = 2V = V_A (This condition is valid only when the driver is present.)
  - $V_{CM\text{-}PECL}$ = 1.2V = V_B (Xilinx requirement.)
- Gain requirements:

$$Gain_{MIN} = \frac{\text{RX Sensitivity (mVppd)}}{\text{Min LVPECL Input Swing (mVppd)}} = \frac{150}{560} = 0.267 \qquad \textit{Equation 8}$$

$$Gain_{MAX} = \frac{\text{Max Input Swing GTX (mVppd)}}{\text{Max LVPECL Input Swing (mVppd)}} = \frac{2000}{2460} = 0.813 \qquad \textit{Equation 9}$$

$$Gain_{MIN} \le Gain \le Gain_{MAX} \qquad \textit{Equation 10}$$

It is generally preferable to have the highest gain because this ensures operation and provides margin for this simple analysis. LVPECL swing numbers are from the *Analog Devices ADCLK944* data sheet [Ref 8].

Given/Known

- VTTRX = 1.2V, V_{PECLCM} = 2V, R_{term} = 50Ω
- Open circuit Thevenin voltage (OCT V) = 1.3V
- Open circuit Thevenin resistance (Z_{in}) = 50Ω
- Target V_{ICM} = 0.7V – 1.2V, VCC_{PECL} = 3.3V

Calculations

A. Theoretical

1. Equation for Z_{in}:
   Using Thevenin's theorem:

$$Z_{IN} = [(R_4 \parallel R_{term}) + R_3] \parallel R_1 = 50\Omega \qquad \textit{Equation 11}$$

Figure 9 shows a Thevenin equivalent network of Figure 8 to calculate Z_{in}.

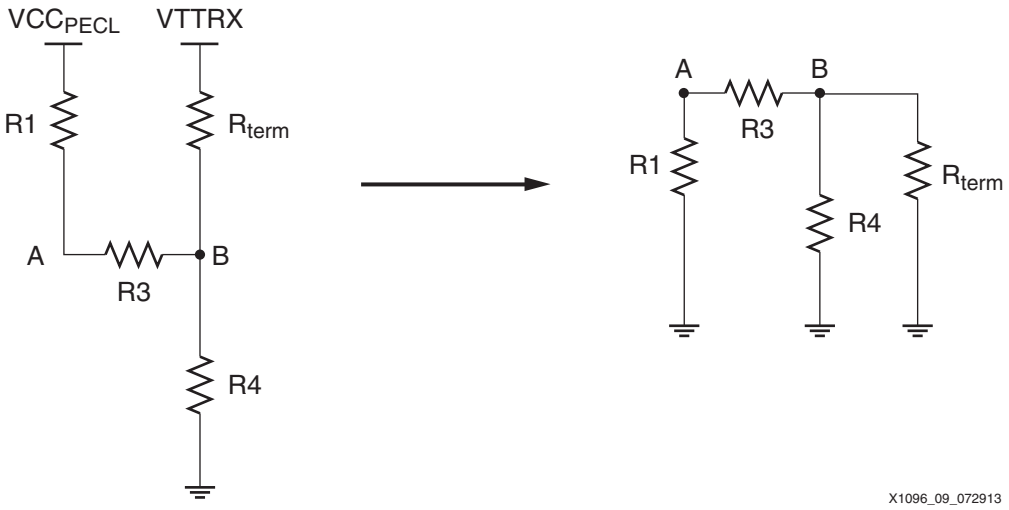

Figure 9: **Thevenin Equivalent Network to Calculate Z_{IN}**

2. Determine values for R_3 and R_4. It is assumed that:

$$R_3 = 50\Omega \quad \text{Equation 12}$$

$$X = [R_3 + (R_{term} \parallel R_4)] > 55 \quad \text{Equation 13}$$

The objectives are for the value of X to be greater than 50Ω, and the parallel combination of R_1 and X should be 50Ω. To be as close to 50Ω as possible, set X > 55Ω so there is some room if R_1 turns out to be a very high number.

When the LVPECL driver is connected:

- V_A = 2V (Use the value for V_A when the driver is connected in order to know the resistance of R_4 in a "real operational" state.)
- From the Xilinx RX requirement, V_B = 1.2V.

Using the preceding information, the value for R_4 can be determined using Kirchhoff's current law (Equation 14):

$$\frac{V_A - V_B}{R_3} + \frac{VTTRX - V_B}{R_{term}} = \frac{V_B}{R_4} \quad \text{Equation 14}$$

$$\frac{0.8}{50} + \frac{1.2 - 1.2}{50} = \frac{1.2}{R_4} \quad \text{Equation 15}$$

$$R_4 = 75\Omega \quad \text{Equation 16}$$

After substituting the values of R_3, R_{term}, and R_4 in Equation 13, the result is that X = 80Ω.

3. Determine gain:

$$Gain = \frac{R_{term} \parallel R_4}{(R_{term} \parallel R_4) + R_3} \quad \text{Equation 17}$$

$$Gain = 0.375 \quad \text{Equation 18}$$

4. Determine the DC input common mode to the receiver (line common mode):

$$V_{ICM} = \left(\frac{V_{CM-PECL}}{R_3} + \frac{VTTRX}{R_{term}}\right) \times (R_4 \parallel R_3 \parallel R_{term}) \quad \text{Equation 19}$$

$$V_{ICM} = 1.2V \quad \text{Equation 20}$$

B. Using Standard 0402 (1005 Metric) Resistor Values for R_3 and R_4

Note: For more information, refer to the DigiKey resistor values [Ref 7].

First iteration:

R_3 = 50Ω

R_4 = 75Ω

Check if OCT V is 1.3V

1. Recalculate X with the new R3 and R4 values:

$$X = 80\Omega \quad \text{Equation 21}$$

2. Recalculate Gain:

$$Gain = 0.375 \quad \text{Equation 22}$$

3. Recalculate V_{ICM}:

$$V_{ICM} = 1.2V \quad \text{Equation 23}$$

4. Determine V_B when OCT V = 1.3V:

   The calculation of V_B is based on the condition that, if OCT V is held at 1.3V, the presumed voltage at V_B supports the configuration with the resistor values selected and calculated.

$$V_B = \left(\frac{OCTV}{R_3} + \frac{VTTRX}{R_{term}}\right) \times (R_4 \parallel R_3 \parallel R_{term}) \quad \textit{Equation 24}$$

$$V_B = 0.937V \quad \textit{Equation 25}$$

5. Calculate R_1 assuming OCT V = 1.3V:

$$R_1 = \frac{V_{CCPECL} - OCTV}{OCTV - V_B} \times R_3 \quad \textit{Equation 26}$$

$$R_1 = 275.8\Omega \quad \textit{Equation 27}$$

   Using standard 0402 (1005 Metric [Ref 7]) resistor for R_1

$$R_1 = 270\Omega \quad \textit{Equation 28}$$

6. Calculate Z_{in} using Equation 11:

$$Z_{in} = 61.7\Omega \quad \textit{Equation 29}$$

Second iteration:

With the calculations in the first iteration, Z_{in} far exceeded the expected value. Adjusting the resistor network so that conditions are met:

Let $R_3 = 40\Omega$ and $R_4 = 40\Omega$. Using 0402 (1005 Metric [Ref 7]), the values are:

- $R_3 = 39\Omega$
- $R_4 = 39\Omega$

Check if OCT V is 1.3V

1. Recalculate X:

$$X = 60.91\Omega \quad \textit{Equation 30}$$

2. Recalculate Gain:

$$Gain = 0.359 \quad \textit{Equation 31}$$

3. Recalculate V_{ICM}:

$$V_{ICM} = 1.05V \quad \textit{Equation 32}$$

4. Determine V_B:

$$V_B = 0.804V \quad \textit{Equation 33}$$

5. Recalculate R1:

$$R_1 = 157.3\Omega \quad \textit{Equation 34}$$

   Using standard 0402 (1005 Metric [Ref 7]) resistor for R1:

$$R_1 = 160\Omega \quad \textit{Equation 35}$$

6. Calculate Z_{in} using Equation 11:

$$Z_{in} = 44.1\Omega \quad \textit{Equation 36}$$

OCT V with 160Ω = 1.293V

Table 4 shows the differences between the expected GPON values and actual values.

Table 4: **Expected GPON and Actual Values**

Parameter	Expected Value	Actual Value
OCT V	1.3V	1.293V
OCT Z_{in}	50Ω	44.1Ω
V_{ICM}	0.7–1.2V	1.05V
Gain	0.267–0.813	0.359

The desired values for OCT V and V_{ICM} are very close to the actual values. There is no performance degradation between 0.7V and 1.2V V_{ICM}. Ideally, OCT Z_{in} should be as close to 50Ω as possible, but with GPON line rates being very low, the reflections due to impedance mismatch should not be a major issue.

Even if the V_{ICM} was close to 1.2V, the RX could have tolerated a TX launch amplitude of 2000 mVpp difference. The reason for this is that the gain due the resistor network is 0.36, which causes a 64% reduction of the signal from the TX to the RX.

Conclusion

The 7 series FPGAs GTX transceivers can be used in DC-coupled applications if the guidelines presented in this application note are followed.

References

1. *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS182)
2. *Zynq-7000 All Programmable SoC (XC7Z030, XC7Z045, and XC7Z100): DC and AC Switching Characteristics* (DS191)
3. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
4. *Introduction to LVDS, PECL, and CML Rev. 1*; Maxim Integrated pdfserv.maximintegrated.com/en/an/AN291.pdf
5. *Interfacing Between LVPECL, LVDS, and CML*; Texas Instruments www.ti.com/lit/an/scaa056/scaa056.pdf
6. *Interfacing Between LVPECL, VML, CML, and LVDS Levels*; Texas Instruments www.ti.com/lit/an/slla120/slla120.pdf
7. DigiKey resistor values: www.digikey.com/scripts/dksearch/dksus.dll?FV=fff40001%2Cfff800e9%2C400004%2C142c1639&vendor=0&mnonly=0&newproducts=0&ptm=0&fid=0&quantity=0&PV3=2
8. *2.5 V/3.3 V, Four LVPECL Outputs, SiGe Clock Fanout Buffer*; Analog Devices www.analog.com/static/imported-files/data_sheets/ADCLK944.pdf

Appendix

I_{DCIN} and I_{DCOUT} Table

Table 5 is a quick reference for the I_{DCIN} and I_{DCOUT} current limits. For the most up to date information, refer to the data sheets [Ref 1] [Ref 2].

Table 5: **I_{DCIN} and I_{DCOUT} limits**

Symbol	Description	Condition	Maximum Current Allowed (mA)
I_{DCIN}	DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V	R_{term} = AVTT	12
		R_{term} = GND	6.5
I_{DCOUT}	DC output current for transmitter pins DC-coupled $V_{MGTAVTT}$ = 1.2V	R_{term} = AVTT	12

Testing Conditions

The tests were performed on multiple -2 devices. Table 6 shows the voltages and temperature conditions.

Table 6: **Testing Conditions**

Conditions	Values
V_{min}	1020 mV
V_{nom}	1050 mV
V_{max}	1080 mV
T_{min}	–36°C
T_{nom}	40°C
T_{max}	100°C

The testing was also done over multiple line common mode voltages of the system.

1. Line Rate:
   a. LPM = 11.3 Gb/s
   b. DFE = 12.5 Gb/s
2. Channel (Swing > 150 mVpp differential)
   a. LPM ~ 11 db
   b. DFE ~ 16 db
3. Channel (Swing = 150 mVpp differential)
   a. LPM = KC724 board trace, no added trace

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
09/13/2013	1.0	Initial Xilinx release.
01/10/2014	1.0.1	Updated table references after Figure 3.

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